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Joe Sanzio, director of systems engineering and quality assurance at Stratus Technologies.

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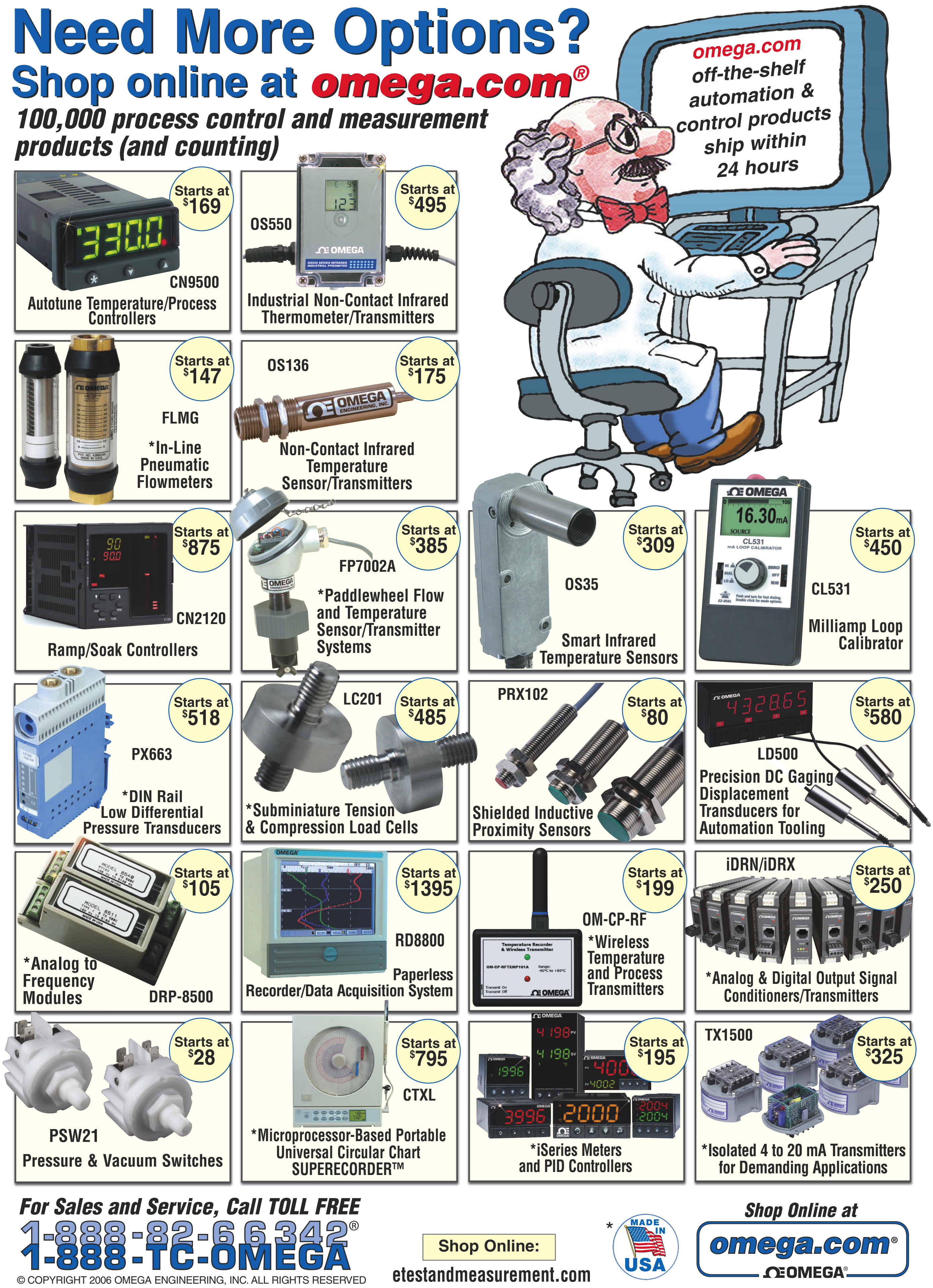

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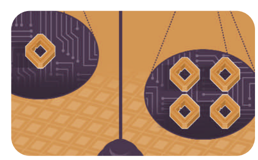

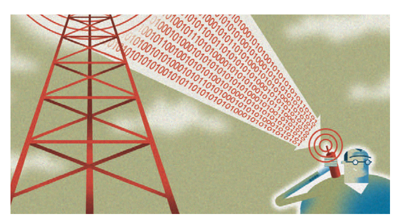

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Too much convergence

"Convergence" was a key theme at the IEEE Microwave Theory and Techniques Society's MTT Wireless Week 2006, held in San Diego January 16–20. Fawzi Behmann, director of strategic marketing at Freescale Semiconductor, addressing a January 16 press conference, discussed "convergence challenges" for next-generation wireless networking. Consumers, he suggested, will be demanding a convergence of ease of use, reliability, and security within devices that provide a convergence of voice, data, and audio and video functionality.

RICK NELSON, CHIEF EDITOR

Product introductions at the show also dealt with convergence. The convergence of RF and mixed-signal circuitry within single products is one factor that prompted Keithley Instruments to launch a new line-up of RF instruments: a signal generator, a signal analyzer, and an RF power meter. Walter Strickler, Keithley director of marketing for wireless/RF business, cited ease of use as a key feature that will make the instruments attractive to engineers facing RF measurement challenges for the first time.

Convergence is good for consumers but challenging for engineers and show organizers.

For its part, Agilent Technologies addressed the convergence of RF, IF, and data-conversion functionality within a single semiconductor device. Agilent application specialist Mark Lombardi explained that with such levels of integration, access to analog I/Q signals is disappearing, although the need to make I/Q measurements is not. Agilent's solution? Porting its 89600 Series VSA (vector signal analysis) software to its line-up of logic analyzers, which engineers can then use to monitor the flow of digital I/Q data across the buses connecting RF and base-band chips.

The Wireless Week show itself helped to demonstrate the limits of convergence. To constitute the week's events, the IEEE Radio and Wireless Symposium, the IEEE Topical Workshop on Power Amplifiers for Wireless Communications, the 6th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, and 125 exhibitors all converged on San Diego. Event general chair Fred Schindler expressed his satisfaction at the registration of about 2000 registrants attending 306 peer-reviewed technical papers. But the technical programs, widely dispersed within the convention-center/hotel complex, seemed to leave little opportunity for attendees to get hands-on experience with the Keithley instruments, Agilent software, and other new products on display.

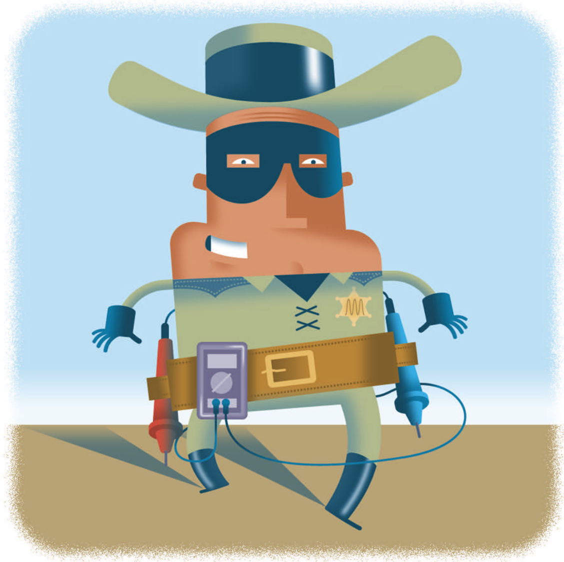
Let's hope that as the "warm weather show" travels to Long Beach, Orlando, and then back to San Diego over the next three years, the organizers will add sufficient breaks within the technical programs to encourage hands-on experience on the exhibit floor. T&MW

Contact Rick Nelson at rnelson@tmworld.com.

TESTVOICES

[An exclusive interview with a test engineer]

The lone test ranger



DANIEL GUIDERA

Bill Drago is a senior engineer at L-3 Communications Narda Microwave-East Division (Hauppauge, NY), which produces passive and active microwave components and subsystems. Products include amplifiers, filters, couplers, transceivers, multiplexers, isolators/circulators, up- and downconverters, channel amplifiers, power dividers, and combiners. Martin Rowe recently spoke with Drago about his work, which covers frequencies from DC to 30 GHz.

Q: What is your role in test?
A: I am the sole engineer at my division responsible for developing and maintaining automated test systems. I support design engineering and production. I define the test plans, configure test systems, write code, and train engineers and technicians on how to use the systems.

Q: What does a typical test system look like?
A: All of the systems I configure for engineering use benchtop equipment such as microwave sources, spectrum analyzers, vector network analyzers, power supplies, temperature sensors, and a digital I/O interface. Most equipment connects to a PC through an IEEE 488 port. The digital I/O module uses a USB port. We're always moving equipment around the lab, so engineering test systems must be flexible. In addition, I often build virtual control panels to control devices under test, which typically contain RS-232, RS-485, or I^2C interfaces.

Q: What do your systems measure?
A: Typically, we measure gain, frequency response, return loss, and phase. In a recent test, I had to measure the response of an oscillator while we struck it with a hammer. It's a requirement for a military standard. I didn't automate the hammer movement, but I did automate the data processing that followed the impact. I spend my time automating data capture so the design engineers can analyze the results. I often need to quickly configure a data-acquisition system that will make measurements over a weekend and store the data.

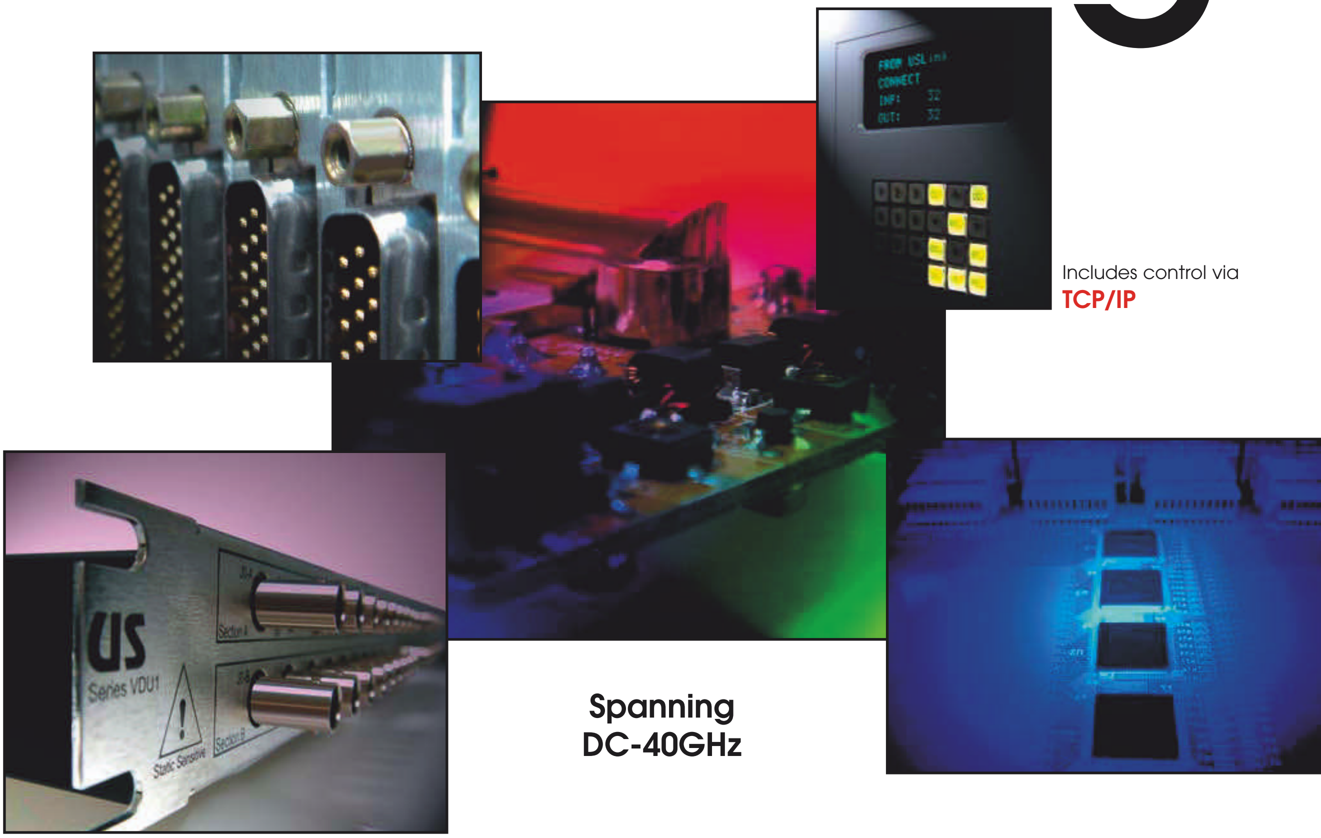
Q: How do you support production?
A: Although I spend most of my time supporting engineering, production is my first priority. I supply and support production test systems. On a recent project, the unit under test was a portable spectrum analyzer for cell-phone towers. I designed the test system so that if a unit failed halfway through its 30 tests and the unit needed repair, the system knew which tests the unit had already passed. It didn't have to start from the beginning of the test sequence, but I gave the technician the option of re-running a test.

Q: How do you get a product ready for production?
A: Once a product is ready for production, I take a subset of the engineering tools I developed and use them in an automated test system. To save time, we may use multiple signal sources so that we don't have to use microwave switches. Not all product test systems are built into racks. Some production systems sit on a bench for years. It depends on the budget.

Q: What are the most significant challenges you face?
A: Keeping up with demand is number one. Engineers come to me with test requirements and they need systems right away. Sometimes, they don't really know what they want, and I have to help them define their tests. I rarely have time to produce code with error checking because the engineers just need a system quickly. I've learned how to produce quality code. I know where not to go when writing code. Another challenge comes in trying to figure out how to program an instrument. Test equipment makers can help by improving their documentation. T&MW

Every other month, we will publish an interview with an electronics engineer who has test, measurement, or inspection responsibilities. If you'd like to participate in a future column, contact Martin Rowe at mrowe@tmworld.com.

Switching?



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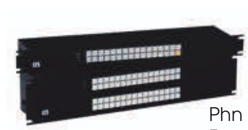

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FEI and PDF Solutions collaborate on defects analyzer

Designed to provide faster access to 3-D defect data and images, a new technique from FEI and PDF Solutions integrates PDF's Characterization Vehicle (CV) infrastructure and FEI's Defect Analyzer 300HP DualBeam system for automated in-fab defect analysis. The companies report that the first combined solution was recently delivered to a US-based microprocessor developer and foundry.

The new integrated flow accelerates yield ramps of deep-submicron semiconductors by speeding root-cause analysis of defects. This provides better control over advanced processes, as well as improved yields, reduced time-to-market, and significantly reduced process development costs, according to the vendors.

In the integrated flow, PDF Solutions' short-flow CV test chips are run through the factory, where electrical tests are performed to identify subsurface failures. Once the analysis software identifies failures, it works with the voltage contrast capabilities of the FEI DA 300HP to pinpoint the location of the failures on the wafer to within a fraction of a micron. Defects are then cross-sectioned by the DA 300HP, resulting in a detailed subsurface image of the failure location and of the failing structure. The image enables engineers to identify the cause of failures and validate potential process changes to determine those that reduce failure rates to an acceptable level. www.feicompany.com; www.pdf.com.

Partners to develop at-speed test

Mentor Graphics has announced a joint development agreement with STARC (Semiconductor Technology Academic Research Center), a research and development consortium co-founded by 11 Japanese semiconductor companies. The joint effort will focus on new at-speed delay-test methodologies for IC designs that aim to improve the detection of small delay defects during manufacturing test. The partnership seeks to fulfill delay-defect detection requirements from STARC and its client companies by incorporating new technologies into Mentor's automatic test-pattern generation IC test tools.

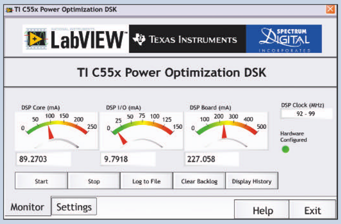
"STARC's mission is to seek out new and effective technologies through joint research between universities and the industry, in order to achieve breakthroughs in semiconductor technologies," said Yasuo Sato, senior manager of the Test Methodology Group at STARC. "As our member companies move to 90- and 65-nanometer technologies, improving manufacturing test is a critical requirement. We believe that this partnership with Mentor will satisfy that requirement and will result in a breakthrough at-speed test methodology."

"The proposals from the STARC consortium for improving small delay-defect detection coincides with Mentor's development efforts in the area of at-speed test-pattern generation," said Robert Hum, VP and GM for the Design Verification and Test Division at Mentor Graphics. "We are extremely pleased to be working closely with STARC and look forward to continuing this development partnership to provide real solutions for STARC and our customers." www.mentor.com; www.starc.jp.

Editors' CHOICE

DSP apps get battery-life boost

The Texas Instruments TMS320C55x Power Optimization DSP Starter Kit (DSK) provides an integrated set of power-estimation and measurement tools, including power-monitoring capability from National Instruments (www.ni.com). Intended to help developers plan, analyze, and optimize real-time power consumption for products containing TI's C55x devices, the DSK also includes TI's Code Composer Studio IDE v3.1 tools, DSP/BIOS Kernel v5.20 software, and a C5509A-based target board with onboard emulation and board-support libraries from Spectrum Digital (www.spectrumdigital.com).



The kit helps developers measure power consumption through real-time profiling of application code, eliminating the need for separate oscilloscopes and current probes. Developers can cycle their designs through profiles over several days to determine the effects of active and stand-by modes on battery life. The integrated NI power-analysis hardware delivers power-monitoring and triggering functionality via a USB interface. TI offers daughter cards to provide for additional features, including fingerprint sensors, LCDs, codecs, and multichannel ADCs and DACs.

Base price: $495. *Texas Instruments, www.ti.com/powerefficientdevices.*

Spin-off gets its name

Agilent Technologies has selected a name for its upcoming semiconductor test spin-off company. The name Verigy will be used when the company separates from Agilent, and it will carry the tagline, "the brilliance of innovation."

The Verigy name is built from the Latin prefix "veri-" ("true, genuine"), which is the root of "verification," and so ties the name to the test business. The "-gy" suffix comes from the combining form "-logy," meaning the name of sciences or bodies of knowledge, as in biology and geology.

"Verigy is emerging from a powerful historical lineage, a direct line from both Hewlett-Packard's standards of integrity and innovation and Agilent's premier measurement business," said Jack Trautman, president of Agilent's Semiconductor Test Solutions business. "This name captures the spirit of our spin-off organization—proven, responsive, energetic, innovative."

On August 15, 2005, Agilent announced plans to spin off its Semiconductor Test Solutions (STS) business, consisting of the system-on-chip and system-in-package (SOC/SIP) and memory-test areas. The spin-off is expected to take place as soon as is practical this year. Agilent's target is to complete an initial public offering of Verigy near mid-2006 and to complete the spin-off by the end of October. www.agilent.com.

CALENDAR

OFC/NFOEC, March 5–10, Anaheim, CA. Sponsored by Optical Society of America, IEEE, Telcordia. *www.ofcnfoec.org.*

International Reliability Physics Symposium, March 26–30, San Jose, CA. Sponsored by IEEE Reliability Society, IEEE Electron Devices Society. *www.irps.org.*

Vision Show East, May 9–11, Boston, MA. Sponsored by Automated Imaging Association. *www.machinevisiononline.org.*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Big screen, big numbers

Editors' CHOICE

The first thing you notice about the DPO7000 series of oscilloscopes is the large, 12.1-in. touch-screen display. The three models in the series (500 MHz, 1 GHz, and 2.5 GHz) can move 250,000 waveforms/s to that screen, which means they can catch most signal anomalies. The deep memory (10 Msamples to 40 Msamples, depending on the numbers of channels) let the scopes run at full sample rate all the time. In "fast acquisition" mode, the scopes store 1000 samples and display them in near real time.

The DPO7000 series features an A/B trigger system that lets you build qualified triggers based on digital bit patterns as well as traditional timing and level conditions. The scopes can also trigger based on bit patterns of low-speed serial buses such as I^2C, RS-232, and the automotive CAN and LIN buses. The DPO7000 can decode packets on the CAN and LIN buses as well. Software applications include mask testing for USB and Ethernet compliance and power analysis for testing switching power supplies.

The DPO7000 scopes come with five USB ports, an IEEE 488 port, and a CD/RW drive so you can store data on a CD-ROM. Memory options increase memory by a factor of five over base models.

Base prices: 500 MHz—$14,000; 1 GHz—$17,900; 2.5 GHz—$24,900. *Tektronix, www.tektronix.com.*

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2005 efforts suggest 2006 ATE and DFT trends

THE SEMICONDUCTOR ATE industry will spend 2006 adjusting to the product innovations and organizational changes that were initiated in 2005. EDA vendors are working to speed test generation, enhance diagnostics, improve fault coverage, and derive yield-enhancement data from the results of scan-based test.

For SOC test, Advantest has claimed success with its T2000 OpenStar system, despite the lack of participation of other SOC ATE vendors in the OpenStar program. (RFIC tester maker Roos Instruments does participate.)

Fusion EX is one of several configurations that let customers tailor the Fusion architecture to their needs.
Courtesy of LTX.

My colleague Jeff Chappell at *Electronic News* (Ref. 1) reports that the T2000 achieved 36% market share in the first half of last year.

Other SOC test participants include Agilent and LTX, who continue to support the single-platform approach they have pioneered for more than five years, Agilent with the 93000 and LTX with Fusion. But despite the single-platform approach, neither company is standing still as they tweak their platforms to optimize cost-effectiveness.

Agilent, whose semiconductor test operation will emerge as Verigy after a mid-2006 spin-off and IPO, introduced last year its InstaPin per-pin licenses for 93000 Pin Scale digital cards, which let customers cost-effectively allocate test capability. For its part, LTX last year debuted 40-slot MX and 80-slot EX systems to complement its 20-slot Fusion CX system.

As Agilent and LTX continue evolving 93K and Fusion, Credence Systems is consolidating its Sapphire technology, acquired with the 2004 NPTest acquisition, into its product portfolio, phasing out its Octet and Quartet platforms. The Sapphire line-up now includes the NPTest-derived Sapphire S platform as well as the Sapphire D-10, a low-cost system introduced in July that offers CompactPCI compatibility.

In addition, Teradyne is expanding its FLEX lineup, now available in microFLEX and ultraFLEX configurations, and the company recently worked with Cadence Design Systems to ensure smooth interfaces between FLEX platforms and Cadence Encounter Test tools (see box below).

In other EDA activity, Synopsys has recently enhanced TetraMAX to speed up ATPG runtime performance and to add a new waveform debugger that helps designers quickly isolate and correct design-for-test problems.

Mentor Graphics introduced its YieldAssist diagnostic tool, which allows semiconductor manufacturers to harvest device failure information from wafer sort to adaptively improve manufacturing-test quality.

A key goal of getting ATE systems to work well with EDA tools like Encounter Test, TetraMAX, and YieldAssist is "getting more out of test"—that's the theme of the 2006 International Test Conference, which is scheduled to commence October 22 in Santa Clara and which will provide the ideal time to see how well ATE and EDA vendors have built on their 2005 momentum. T&MW

REFERENCE

1. Chappell, Jeff, "2005: A Time of Change for ATE," *Electronic News*, December 30, 2005. www.electronicnews.com.

Low-inductance socket

Advantest has developed a low-inductance IC socket for high-volume production test of high-speed packaged devices. At 0.4 nH or less, the socket achieves a 73% reduction from the self-inductance value of the company's previous model. It supports BGA, FBGA, and CSP packages having a 75-mm, 0.8-mm, 1-mm, or 1.27-mm ball pitch. www.advantest.com.

Teradyne and Cadence validate flow

Teradyne FLEX platforms running IG-XL software now support Cadence Design Systems Encounter True-Time Delay Test patterns in industry-standard STIL or WGL format and Encounter Diagnostics Chip Pad Pattern (CPP) format, establishing a validated flow for test and yield diagnostic information between FLEX systems and Encounter Test software. Teradyne and Cadence also validated a path from Teradyne ATE to Encounter Diagnostics to help customers resolve ATE failures and enhance their yields. www.cadence.com, www.teradyne.com.

Credence appoints executive chairman

Credence Systems has announced that Dave House, a 40-year veteran of the computing, communication, and semiconductor industries with 22 years in management positions at Intel, was appointed as executive chairman of Credence's board of directors, effective December 9, 2005. House succeeds Dr. Graham Siddall, who retired as executive chairman on October 31, 2005. www.credence.com.

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A need for speed

MANY INSPECTION systems work well with standard TV-type cameras that operate at 30 frames/s. But as production-line speeds increase, engineers must look to digital cameras that offer higher image rates, often between 60 and 120 frames/s. A change from an analog camera to a high-speed digital camera, however, involves more than substituting one camera for another.

Engineers have often mated analog-output cameras with inexpensive PC-based frame grabbers that digitize video signals. High-speed digital cameras, though, rely on standard digital interfaces such as USB, FireWire, or Gigabit Ethernet that PC vendors supply or that designers can add to a PC at low cost. (The Automated Imaging Association's proposed "GigE Vision" standard will operate at about 800 Mbps, which will accommodate a 2-Mpixel camera at 30 frames/s or a 1-Mpixel camera at 60 frames/s.)

The GE Gigabit Ethernet series of cameras can operate as fast as 200 frames/s with a resolution of 659x493 pixels. Such cameras find use on high-speed production lines and in motion-analysis equipment. Courtesy of Prosilica.

Another AIA camera-interface standard, Camera Link, requires a compatible frame grabber, available from vision-equipment suppliers. If you have an application that requires more than 60 frames/s from a megapixel camera, Mark Butler, product manager at Dalsa, recommends that you consider Camera Link for real-time imaging, because it allows for data rates as high as 5.4 Gbps.

These digital-communication standards impose new limits on the distances between cameras and host computers, an aspect of system integration that some engineers may overlook at first. "Gigabit Ethernet lets you put a camera about 100 m from a host PC," said Ken McDonald, senior applications engineer at JAI Pulnix. "But Camera Link gives you a 10-m distance between a camera and a PC, USB limits that distance to 15 ft, and FireWire sets a limit of about 10 ft."

The use of high-speed cameras also affects lighting and lens choices. "When a camera operates at 30 frames/s, you have a 33-ms exposure time," McDonald said. "But at 100 frames/s you have only a 10-ms exposure time, so you need more than a threefold increase in light intensity to get the same number of photons to the high-speed camera's sensor."

A lens with a lower f number can help gather more light with its aperture fully open. "But when you open the aperture, you also decrease the depth of focus, or depth of field," explained Marty Furse, CEO of Prosilica. "That means your system may not properly focus on all the features it must inspect." To obtain more light without changing lenses or lens settings, you can employ light sources such as LEDs or xenon flash lamps that produce brief bursts of high-intensity light.

If lighting changes and lens adjustments still don't provide enough light, Furse said you can consider changing the gain of their digital cameras. But a gain increase also may increase noise in a video image. Thus, if you plan to change gain settings, you should specify low-noise cameras—those with a high signal-to-noise ratio. T&MW

For more information about digital interfaces, see "Camera Link and GigE improve image speeds," p. 52.

Color for in-line vision

PPT Vision has introduced two intelligent color cameras for in-line applications. The Impact T28, with 1600x1200-pixel resolution, handles high-accuracy color verification, label inspection, and real-time part sorting. The Impact T24 offers 1024x768-pixel resolution. With an onboard image processor and real-time I/O and Ethernet communications, both products are designed to provide 100% quality verification. www.pptvision.com.

Sensors inspect shapes

Designed for inspecting the presence and shape of defined areas, the PresencePlus P4 Area vision sensors from Banner Engineering perform multiple analyses simultaneously at speeds up to 10,000 parts/min at a resolution of 128x100 pixels. The P4 Area 1.3 version operates to 1200 parts/min, offers a resolution of 1280x1024 pixels, and includes gray-scale and blob-analysis tools for rendering pass-fail judgments. www.bannerengineering.com.

Geometric pattern finding

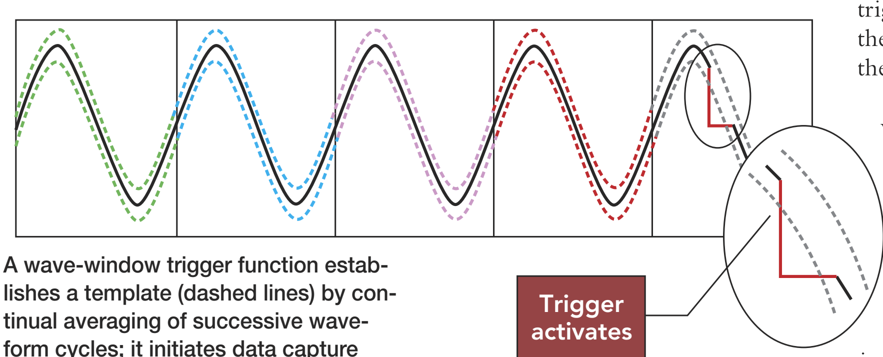
Many vision applications require a pattern-finding tool (PFT), but PFTs based on normalized cross-correlation (NCC) techniques suffer major drawbacks. The white paper "How to Evaluate a Geometric Pattern-Finding Tool," from Dalsa Coreco, describes a geometric PFT that can tolerate many types of image degradation, including rotation, scaling, nonlinear brightness changes, occlusion, and objects touching one another. The paper describes how to select and employ geometric PFTs. www.coreco.com.

WEBCAST

Optimize resolution, sampling rate, and memory

Eight-bit scopes are ubiquitous measurement workhorses, but in many cases, you might benefit from flexible alternative instruments that let you tune bandwidth, resolution, sampling rate, and recording time to the specific needs of an application. In the Webcast "When 8-bit scopes aren't enough," Boyd Shaw, product manager for Yokogawa, describes what he calls "hybrid instruments"—ones offering high resolution (up to 16 bits), isolated inputs, very long memory for long-term recording, and support for a variety of signal inputs—and he describes how they differ from oscilloscopes and data recorders (Ref. 1).

Shaw shows you how to tailor instrument performance for long acquisition times or high sampling rates, and he describes a dual-capture scheme that lets you optimize both. He recommends selecting a bandwidth three times the highest frequency component of the signal you want to observe, adding that you'll need seven or more times your signal's bandwidth if you need to accurately capture pulse edges.



A wave-window trigger function establishes a template (dashed lines) by continual averaging of successive waveform cycles; it initiates data capture when a measured signal's value exceeds the template limits.

In addition, Shaw describes several triggering mechanisms that can be beneficial in the types of applications that hybrid instruments serve. He covers edge, timer, pulse-width, and serial-bus triggers, and he describes combination triggering—for example, triggering on the *n*th occurrence of condition B after the first occurrence of condition A.

Shaw also describes how to use a wave-window trigger (**figure**), which can be beneficial in tracking down AC-power-line abnormalities such as sags, surges, and frequency fluctuations. An instrument capable of wave-window triggering generates a real-time "ideal waveform" template based on continual averaging of previous waveform cycles; it compares each new waveform to the template it has created and triggers the instrument's capture mechanism when it detects significant deviations.

Rick Nelson, Chief Editor

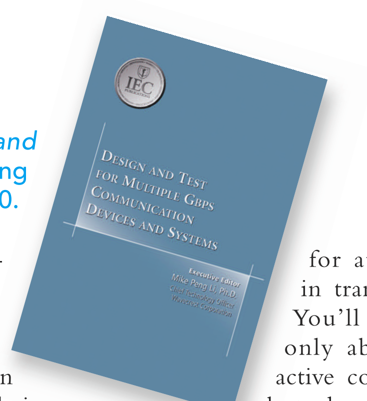
REFERENCE

1. "When 8-bit scopes aren't enough," produced by *Test & Measurement World* and sponsored by Yokogawa's Test and Measurement Div., originally broadcast November 30, 2005. www.tmworld.com/webcasts.

BOOK REVIEW

Papers tell the gigabit story

Design and Test for Multiple Gbps Communication Devices and Systems, Mike Peng Li, executive editor, International Engineering Consortium, Chicago, IL (www.iec.org/pubs), 2005. 497 pages. $80.



If you need a background or an update on the physical-layer technology behind high-speed serial communications, then this book is for you. Executive editor Li has compiled 20 first-rate technical papers into a book that covers the hardware in communications buses such as PCI Express, SerialATA, and XAUI. The papers, written by industry experts, focus on the theory, design, and test aspects of these buses. You'll learn about signal integrity (with a solid emphasis on jitter), eye diagrams, modeling, and measurements.

From reading the papers, you'll understand the tradeoffs in designs and how to decide on a design strategy. For example, "Optimal Use of Signal Conditioning in 40-Gbps Copper Interconnects" teaches how pre-emphasis and de-emphasis in transmitter and receiver circuits compensate for attenuation in transmissions. You'll learn not only about these active components, but also how connectors, PCB traces, and vias affect signal integrity.

As the chief technology officer at Wavecrest, a manufacturer of signal analyzers, Li brings extensive knowledge

Papers tell the gigabit story *(continued)*

of jitter and signal-integrity measurements to this book. He authored or co-authored five of the book's papers, including papers on jitter, its components, and how to evaluate them. He also shows how jitter has a direct relationship to bit-error rate.

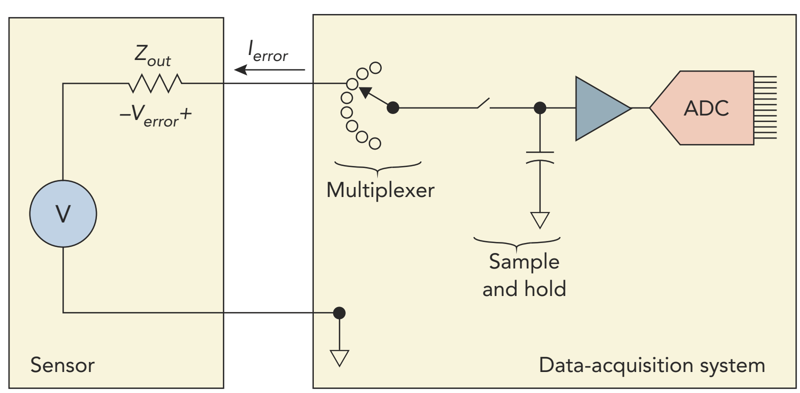
The papers in this book provide you with an abundance of plots, circuit diagrams, and test setups that clearly highlight how transmitters, receivers, clocks, and filters must work together to produce a reliable serial link. None of the papers turns into a product promotion, so you won't get details on how to use a specific product, but you will get an in-depth look at the technology.

Martin Rowe, Senior Technical Editor

DATA ACQUISITION

Charge injection creates measurement errors

Every time a multiplexed data-acquisition system switches channels, it produces a small electric charge that can produce measurement errors. "Users of data-acquisition equipment may have these charge-injected errors and not even know it," said Glenn Fasnacht, senior project engineer at IOtech. "I pay much more attention to this and other measurement problems now that I design data-acquisition systems than I did when I was a user."



Multiplexed data-acquisition systems produce charges that can create error voltages.

When a multiplexed data-acquisition system switches channels, it produces about 4 or 5 pC of charge. If that charge connects to a sensor with a high enough output impedance, it can produce an error voltage (**figure**). Remember that $I = Q/t$. If the 4 pC occurs for 100 ns, it produces 40 µA of current. If your sensor has a source impedance of 100 Ω, the current (I_{error}) and impedance (Z_{out}) will produce an error voltage (V_{error}) of 4 mV.

"The best way to minimize errors from charge injection," noted Fasnacht, "is to use a sensor with a low source impedance." Sensors such as accelerometers, load cells, and even thin thermocouples connected to long wires can have enough output impedance to cause charge-injection errors. Fasnacht recommends that you use a signal-conditioning amplifier or op amp wherever possible, because its low output impedance (typically 1 Ω or less) reduces the error voltage to insignificant levels.

You can download the complete interview with Fasnacht from the online version of this article at www.tmworld.com/2006_02.

Martin Rowe, Senior Technical Editor

INSTRUMENTS

Many tests, many setups

DEVICE UNDER TEST
Broadband differential variable-gain IC amplifiers. The amplifiers are designed to operate at frequencies from DC to 10 GHz with a maximum gain of 27 dB. The amplifiers are used in medical instrumentation and test and measurement equipment.

THE CHALLENGE
Fully characterize the amplifiers under operating conditions such as temperature, power-supply voltage, and input signals. Tests on the amplifier include gain, common-mode rejection, linearity, differential output voltage, total harmonic distortion, and power dissipation. Develop unique setups for each test. Conduct all tests at temperatures of 25°C, 55°C, and 85°C and with supply voltages 4.75 V_{CC} to 5.25 V_{CC} and –4.94 V_{EE} to –5.46 V_{EE}.

THE TOOLS
- Agilent Technologies: Vector network analyzer, network/spectrum/impedance analyzer, transmission/reflection test set, sweep generator. www.tm.agilent.com.
- Anritsu: Microwave power divider. www.us.anritsu.com.
- Picosecond Pulse Labs: Bias insertion tees. www.picosecond.com.

PROJECT DESCRIPTION

Inphi (Westlake Village, CA; www.inphi-corp.com) manufactures broadband amplifiers that require dozens of measurements during design verification. When engineers developed a DC-to-10-GHz differential amplifier, they knew that customers would need these measurements to specify the amplifier. For each of the measurements, principal design engineer Mike Case configured a circuit.

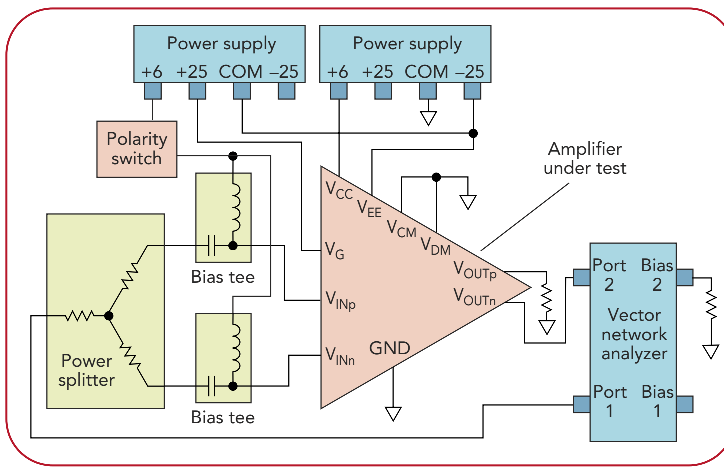
Because of the amplifier's differential design, Case had to measure its common-mode rejection (CMR). The **figure** shows the test setup for CMR measurements. The right-hand power supply provides power to the device under test (DUT), while the left-hand power supply provides a gain-control voltage to the amplifier's V_G pin. The left supply also produces a DC voltage that, through the polarity switch and bias tees, becomes the DC common-mode signal used to bias the AC signal from the vector network analyzer's (VNA's) port 1 output. Case used two network analyzers, switching between them at 100 MHz.

A 100-mV AC signal from the VNA feeds a power splitter that produces two outputs, each of which is 50 mV. The outputs connect to the DUT through phase-matched cables. Case measured the amplifier's output at three gain settings (high, middle, and low). Because the amplifier's common-mode gain is 6 db higher than the value measured by the VNA, Case adds the single-ended gain (6 dB less than the common-mode gain) to the measured CMR. That produces the common-mode rejection ratio measurement.

When Case measured CMR with signals above 10 kHz, the amplifier performed within specifications. But he needed to make CMR measurements with AC signals down to DC, and he still needed to produce a common-mode voltage to measure CMR. The manufacturer of the bias tee, however, specifies the device's low-frequency limit at 10 kHz. Below 10 kHz, Case encountered CMR measurements that didn't make sense. "We expected the bias tee to function like a linear high-pass filter below 10 kHz," he said, "and we assumed that we could compensate for those effects."

The DC common-mode voltages changed unexpectedly when the AC signals went below 10 kHz. The nonlinearity appeared to produce gain errors, which Case also observed while measuring the amplifier's single-ended gain. The bias tees altered the amplitude of the AC signal, which produced the illusion of a nonlinear gain-versus-frequency measurement in the amplifier.

"We attributed the unexpected differences in gain and CMR to a nonlinear inductance in the bias tees below 10 kHz," said Case. As a result, he hasn't yet made CMR measurements below that frequency, except with the common-mode voltage set to 0 V.



Inphi engineers used this setup to measure common-mode rejection in a DC-to-10-GHz differential amplifier IC.

LESSONS LEARNED

If you use an electronic component outside its specified range, you can't always predict how it will perform. When I interviewed Case, he was looking into other methods to make the CMR and single-ended gain measurements with input signals below 10 kHz. He also learned that hysteresis in the bias tees made characterizing them difficult below that frequency because the hysteresis makes them perform nonlinearly.

Martin Rowe, Senior Technical Editor

Hardware design lead Joe Amato uses logic analyzers connected to CPU motherboards so he can monitor bus signals.

DOWNTIME is NOT an option

ENGINEERS AT STRATUS TECHNOLOGIES TEST THEIR FAULT-TOLERANT COMPUTERS TO MAKE SURE THAT CUSTOMER APPLICATIONS NEVER FAIL.

MARTIN ROWE, SENIOR TECHNICAL EDITOR

MAYNARD, MA—If the servers at banks or other financial institutions fail, they may lose your transaction—and your money. If a pharmaceutical company's servers fail, it may lose manufacturing documentation, and regulations may force it to destroy some of its production. If servers used in security systems or other public-safety applications fail, the consequences can be tragic. For these and other mission-critical applications, downtime can cost serious money, lead to legal problems, or compromise public safety.

Organizations that can't afford downtime often turn to Stratus Technologies. Since 1980, Stratus has supplied customers with hardened, redundant, fault-tolerant servers.

Stratus servers not only test themselves during startup and while in operation, but they also report impending problems to Stratus and switch to backup systems before downtime occurs. The servers employ two and sometimes three redundant CPUs to keep applications running even if one CPU should fail—without the user ever knowing that a failure occurred or that a CPU has been replaced. ("Locked in step," p. 26, describes how Stratus servers maintain redundancy.)

Stratus, however, doesn't rely solely on redundancy to keep its systems running. "Availability derived from redundancy alone is the exception, not the rule," said Joe Sanzio, director of systems engineering and quality assurance. Engineers design and thoroughly test CPUs and I/O subsystems to resist failure.

Always up

To run 99.999% of the time, Stratus servers need tests that go beyond those found in other computers. The company's engineers test new designs at every level. They inject hardware and software errors, run the systems at low voltages, and remove CPU modules and I/O subsystem modules, called "slices," from a rack while other slices keep running.

Steve Mango, manager of system development for the company's ftServer products, leads a team of design engineers, half of whom run simulations on Cadence equipment where they perform signal-integrity and timing analysis. In fact, one of the engineers designs only clock circuits because a system's reference clock is the only component that's not redundant. Thus, it must be stable, reliable, and produce clean signals. Each CPU slice contains its own clock, derived from the reference clock.

Stratus engineers work with the ICS PC Clock Division of Integrated Device Technology to design a custom clock-generation chip. As part of a clock circuit's design verification, Mango's staff measures phase noise, cycle-to-cycle jitter, and long-term jitter with a high-bandwidth oscilloscope. "We always need the highest bandwidth oscilloscopes on the market," said Mango. "That's why we rent them. If we purchased these scopes, we'd have to buy a new one for each new project." At the time of my visit, Mango's engineers were evaluating top-of-the-line scopes from Tektronix and LeCroy before deciding which one to rent.

Joe Sanzio, director of systems engineering and quality assurance, oversees hardware, software, and system-level testing.

Engineers also model printed-circuit boards, connectors, sockets, and cables in both the time domain

PHOTOS BY MARK WILSON

and the frequency domain and measure the effects these components have on signal integrity. They use a Tektronix communications signal analyzer with the time domain reflectometer (TDR) module to take single-ended and differential impedance measurements. They use software to operate the instrument as both a TDR and vector network analyzer.

The other half of Mango's engineering team designs and tests CPU motherboards and I/O subsystems. The I/O subsystems hold or connect to disk drives, keyboards, mice, network cards, and other peripherals. These systems must perform far better than most computers. For example, internal buses such as PCI Express must run a bit-error rate (BER) of less than 10^{-15}. Most computers are deemed acceptable if their bus BER reaches 10^{-12}. To achieve such low error rates, engineers optimized Intel's reference design for PCI Express by moving signal lines and reducing crosstalk.

Stratus engineers test CPU motherboards under strenuous conditions. Hardware design lead Joe Amato and others force hardware errors and test how the system responds. Amato adds resistors, coax cable, and microwave attenuators to clock lines to degrade signal quality. He does the same to I/O buses. He measures the altered signals with an oscilloscope and looks for logic errors with logic analyzers

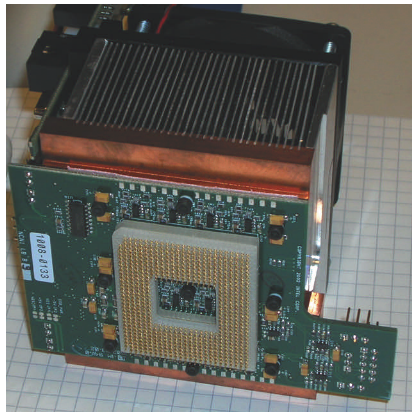


FIGURE 1. A voltage-transient test tool provides access to a CPU's signals.

from Agilent Technologies and Tektronix. For all of these tests, Amato looks for instances where online and offline CPU slices lose lockstep operation.

Amato also tests motherboards under varying voltage conditions. He lowers a board's operating voltage to levels below a processor's specifications to find where hard and soft failures occur.

Onboard diagnostics

In actual operation, a Stratus system's diagnostics will detect a low power-supply voltage before failure occurs, which will force an offline, backup CPU to take over. Mike Kement, design lead for power, mechanical, and compliance, designs circuits that trigger the switchover. Kement designed comparator circuits, based on a voltage reference, that monitor voltages and generate an interrupt that notifies the system of an impending failure. He designs the circuits with enough guardband to ensure switchover without a service interruption. Kement measures the accuracy of the voltage circuits with a Nicolet 12-bit oscilloscope.

Kement also runs power-related tests on CPU and I/O slices. He measures power-supply ripple and noise throughout a board with an oscilloscope. He also tests systems to see how they respond to power-supply shorts and opens. In one test, he shorts a system's 150-A power supply with a 2-in. wide, 0.75-in. long piece of copper to see if it recovers after he removes the short.

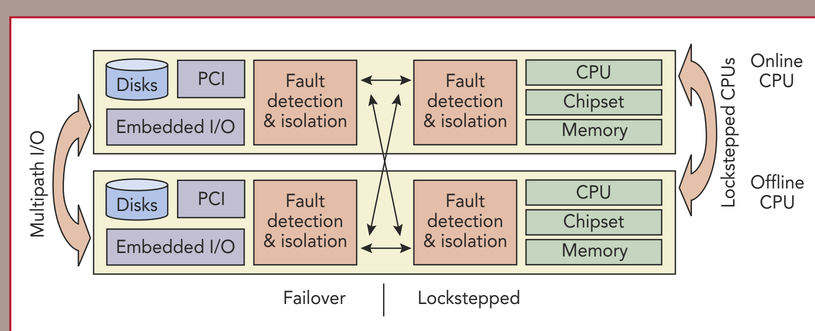
"The shorting bar's resistance, 0.015 mΩ, must be low enough to force the supply into current-limiting mode," Kement said. "Otherwise, the short will function like a load and it will melt from heat." Kement reminisced about how he once tried this test with tweezers. Heat from the current fused the tweezers to the power supply. "We put provisions on our boards for test purposes," noted Kement. "Test points let us place shorts across power pins, such as those on disk drives. We make sure that shorts don't cause system crashes."

Locked in step

A Stratus computer uses two or more CPU "slices" mounted in a rack. An I/O slice contains hard drives and other peripherals, and every slice contains its own power supply. Except for the system clock, every component in a Stratus computer has a backup. The key to this redundancy is called "lockstepping." The **figure** shows two lockstepped CPU slices. When two or more CPUs run in lockstepped mode, the online CPU runs the applications while the offline CPU contains a copy of the online CPU's memory. Thus, it's always ready to assume control should the online CPU fail.

The chipsets keep both CPUs and their memory running in parallel, performing the same operation in perfect synchronization. Fault detection and isolation logic circuits monitor the CPUs for errors and keep the I/O (PCI, USB, hard drives, etc.), called the "failover" side, isolated from the CPUs. Upon detecting a fault, the logic circuit can switch operation from the online CPU to the offline CPU, turning the latter into the new online CPU. Lockstep processing ensures that the system will detect any errors, even transient errors, and survive without losing any data.

If a CPU fails, the backup will notify Stratus. The company will immediately ship a replacement to arrive the next day.—*Martin Rowe*



Stratus servers use two or more CPU modules, called "slices," that duplicate memory contents. Courtesy of Stratus Technologies.

The power applied to a processor directly affects its performance. To monitor voltage transients at the processors, Kement uses a voltage-transient test tool from Intel (**Figure 1**). With the tool, he can measure the power at the processor and he can apply a load to the power supplies and test them. Kement also designs the voltage regulators that supply processor voltages. They step a power-supply's output (typically 5 V) down to a range of 0.9 V to 1.5 V. These voltage regulators also need testing, for which Kement uses Kikusui electronic loads.

As a thermal designer, Kement tests new products with as many as 40 thermocouples to a CPU or I/O slice. A Fluke data-acquisition system collects the data. During a test, Kement controls the power to the chassis' fans with a Xantrex programmable power supply while he measures air flow with an airflow sensor from DegreeC. "We run the thermal tests to make sure that the processors don't enter thermal-throttling mode," Kement stressed. Thermal throttling occurs when a processor senses that its temperature is too high, so it runs at a slower speed to control its temperature. Stratus computers are designed to run cool enough to avoid thermal throttling. Kement adjusts fan voltages to verify that there's enough thermal margin to avoid the condition.

All products also need temperature-cycling testing, which is also Kement's responsibility. He places products in a TestEquity thermal chamber and cycles them from 5°C to 50°C to meet network equipment building system (NEBS) requirements. Stratus servers are qualified to operate in a telecom central-office environment.

In his role as compliance engineer, Kement runs precompliance EMI scans in the lab on all new designs. He uses antennas from ARA Technology and a spectrum analyzer from Agilent Technologies to measure conducted and radiated emissions prior to sending a product to IQS or Curtis-Strauss EMC labs for compliance testing. He also performs power-line tests on all new products. A California Instruments AC power source lets him control mains voltage and inject faults such as dips and other transients. Finally, he conducts ESD tests with a Thermo KeyTek ESD simulator.

MARK WILSON

Steve Mango, manager of ftServer system development, leads a team of design engineers in hardware design and test.

Software tests

Mango, Amato, and Kement come from the hardware side of Stratus, but that's just half of the test story. The rest falls to software and system testing. Software begins with the BIOS, the code that initializes and tests a motherboard and brings it to a state where the operating system can load. A Stratus BIOS is unique because it must initialize two motherboards and bring them into lockstep before the operating system—Windows Server, Linux, or Stratus's own Virtual Operating System (VOS)—takes over. In addition to initializing two or more motherboards, the BIOS performs many system tests.

Dan Lussier is director of firmware and advanced product development. He and others write and test the BIOS code. During boot up, the BIOS checks the motherboards of both the online CPU and the offline CPU. It will enumerate and test the I/O subsystems but make them available to the online motherboard only. If a motherboard failure is imminent, the BIOS will log the failure and activate the offline, backup CPU slice. The BIOS also constantly copies the contents of the online CPU's memory into the offline motherboard in case lockstep breaks and the offline motherboard must take over. Because these systems must always run customer applications, a motherboard can download and upgrade its BIOS without interrupting system operation.

Lussier and others test a BIOS by injecting faults while a motherboard boots. They simulate stuck bits by manipulating registers, and they evaluate how the BIOS responds to those faults. They also perform power failures during a boot to see how the BIOS handles a failed CPU slice.

To inject bit errors into the system, Lussier uses a CPU motherboard's baseboard management control (BMC), which is available through a "back door" command-line interface. Firmware engineers have written scripts that program the BMC to inject errors and report results. The BMC should report any and all hardware errors in a system and it should prevent a motherboard from coming online if it detects a hardware failure during a power-on self-test. "We still perform some BIOS tests by hand," admitted Lussier, explaining that engineers sometimes use switch boxes to inject bit errors. "But we're always looking for ways to automate our tests."

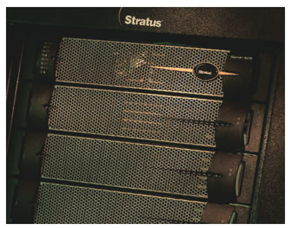
Automation is key to performing repeated system-level tests that can expose stability problems. John McQueeney, manager of platforms and options system test, leads a team of 10 QA engineers who also review designs. They look for ways to automate testing of a new product before they receive it. They test systems following integration of the operating system and any peripherals. McQueeney's team looks at system-level issues. "We test a system to see how the operating system responds to faults," said McQueeney. His engineers look for overall system stability following a fault.

McQueeney's engineers start by injecting single faults at the system level. Some are bit errors in cables while others come from simulated broken communications lines. For example, they use optical switches from Apcon to break optical communications links that carry Ethernet or Fibre Channel packets. If a system test point is suitable, they automate that condition to test it thousands of times. They also inject packet errors and simulate heavy amounts of traffic with either a PC or another ftServer.

"Just because a server keeps running after a single fault doesn't mean it's ready for production," said Joe Sanzio. "We run scripts that force errors to occur thousands of times." Typical errors include parity errors in a memory module.

"If a system repeatedly finds a bit error in the field," added McQueeney "it's taken out of service, so engineers try to force those conditions in the lab to ensure that the system tracks mean time between failures." For example, if a system detects the same error once an hour for 10 consecutive hours, it will notify Stratus to send a replacement part. All motherboards contact Stratus directly, either by sending an e-mail or by dialing through a modem. A customer will receive a replacement slice the next day and technicians will install it without causing a service interruption.

McQueeney's team automates testing wherever possible. They've written scripts to generate network traffic and to initiate simulated faults. Until recently, they used VBScript, but now they use Perl. "We switched to Perl because it's a cross-platform language," said McQueeney. "It runs on Windows, Linux, and VOS. It can also call C-based routines. We wrote the scripts for Windows and we just need to recompile them for Linux and VOS."



Because system restarts are unacceptable, the company's software engineers write their own "hardened" drivers.

The highest level of test responsibility falls to senior QA engineer Henry Ellis, who tests systems with software faults that simulate in-service errors. Using the company's VOS, Ellis runs systems to exhaustion. He focuses on VOS because the customers with the most critical needs use it.

Ellis pushes system resources beyond their designed limits by running more applications than he expects a customer to run. He also runs systems to their limits of memory and disk space to make sure they won't disrupt service. "I look for new ways to introduce trauma," he said proudly. "It's the only way we can fully understand how the customer uses our product."

Peripheral tests

Stratus engineers perform the worst-case tests not only on products they design, but on purchased products, too. Stratus computers use industry-standard components wherever possible. Components include memory modules, hard drives, keyboards, mice, network cards, and other cards that use the PCI, PCI-X, and PCI Express buses. Unfortunately, these products are often out of Stratus' control, so they require constant testing.

Sanzio cited the testing of purchased components as one of the major challenges facing his team of 30 people. For example, he found a memory-module maker who changed to a different IC package. The change was irrelevant to many users, but not to Stratus, for the new parts failed when installed in a Stratus server.

Stratus engineers often uncover design flaws in purchased products. "We bring out the weaknesses because we often test products beyond their specifications," said Mango. "We once uncovered a timing error in a memory module that was sensitive to low power-supply voltages and shared our results with the supplier. After a year of working with the supplier, we dropped the company from our supplier list when the problem remained unresolved."

Firmware changes in purchased products can also affect their functionality in a fault-tolerant environment. When a maker of CD-ROM drives made a firmware change, Stratus systems failed a test that required an offline motherboard to become active. The CD-ROM failed to operate when the system switched to a backup CPU slice.

Crashes caused by poorly written device drivers are a significant cause of system restarts in most computer systems. Because system restarts are unacceptable, the company's software engineers write their own "hardened" drivers. Sanzio noted that Stratus had to modify Intel's drivers for its Gigabit Ethernet adapter cards and Fibre Channel host bus adapters to make them more crash resistant. The company's software engineers also write drivers for USB peripherals that ensure there's no chance that removing a USB device can cause a system crash.

Long-term challenges

Because customers use the company's products for longer periods than do users of general-purpose computers, new Stratus products must maintain complete compatibility with older systems. If a customer's system needs a replacement CPU slice, for example,the new slice must operate with that system's installed peripherals. Often, Stratus also must provide firmware that's not the latest version to maintain compatibility with older products.

Stratus engineers must also contend with issues that affect the entire electronics industry. For example, Sanzio sees compliance with the European Union's new directive on hazardous waste (RoHS) as a serious challenge facing the company. The changeover to lead-free components requires complete qualification tests on every aspect of a product. And as you can see, that's no small task when testing a product where downtime isn't an option. T&MW

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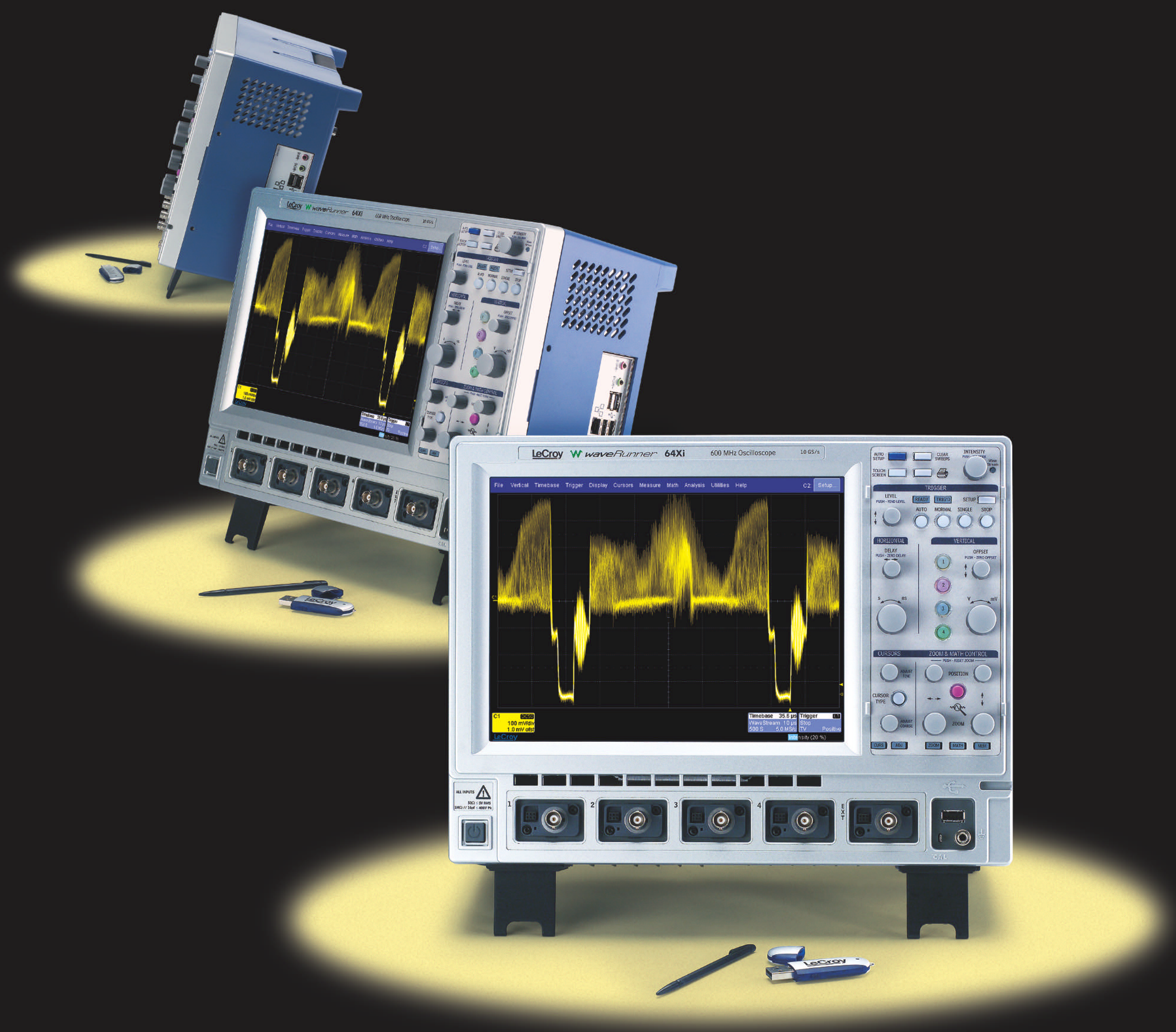

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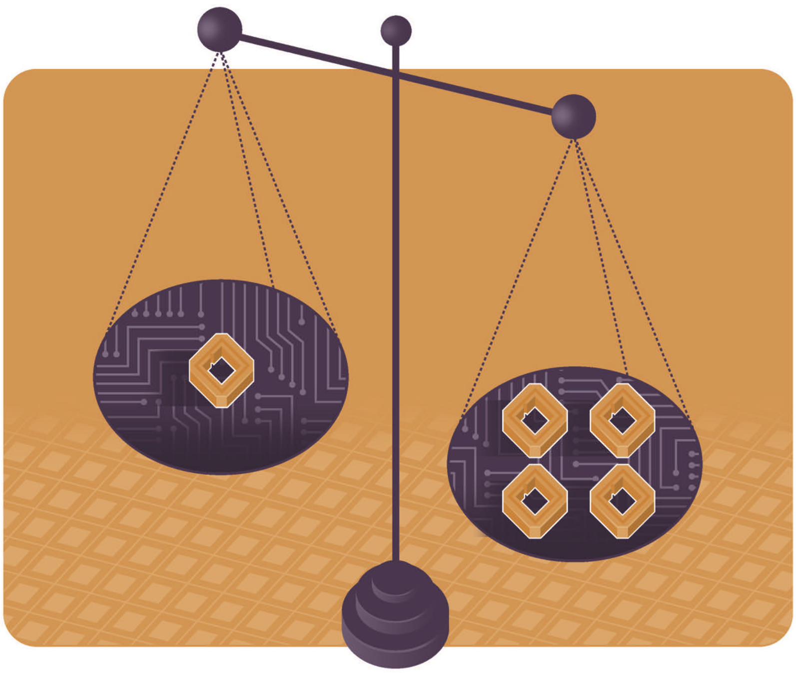
THE CHALLENGE OF MULTISITE TEST



Translating the economic benefits of parallel memory test to non-memory devices.

GREG SMITH, CONSULTANT

It seems simple. If you want to cut the cost of test for an IC, you should double or even quadruple the number of devices you test in parallel. After all, memory manufacturers have proven the value of this technique beyond a shadow of doubt—it's becoming standard practice to test 128 DRAMs in parallel (Ref. 1). Multisite testing has reduced the capital cost of a DRAM test site from $400k in 1997 to about $27k in 2004, allowing test costs for memories to stay constant or even decrease, even though densities have increased from 64 Mbits to 1 Gbit over the same period.

Why shouldn't the same math apply to all devices? To some extent it does, but most test engineers know that things are never as simple as they seem. Memories and SOCs are very different, and analyzing those differences can help you see why increasing the number of test sites may not necessarily result in cost savings on some testers.

In previous generations of non-memory testers, the combination of pin count, BIST/DFT features, and mixed-signal cores in non-memory devices conspired the keep most production test solutions to a maximum of dual site. Most testers did not provide the specialized features that allow the tester to independently synchronize to multiple devices in parallel, robbing efficiency from multisite solutions. Only recently have some ATE manufacturers delivered testers that provide sufficiently high-density digital and mixed-signal instruments and architectures that are capable of supporting massive multisite for non-memory devices.

The two key differences between memory and non-memory devices are test times and total production volumes. Big production runs and long test times make memories ideally suited for massively parallel testing. A memory tester equipped with 128 sites testing a 1-Gbit memory with a 128-s test time will have an output of about 3600 units per hour (UPH). A non-memory tester with four sites testing a device with a 4-s test time has the same throughput. An attempt to reduce test cost for this device by going to a 16-site test would theoretically produce 14,400 UPH, but other facets of production are likely to limit the payback from creating a massive multisite test solution.

Multisite efficiency

The relative efficiency of testing memories and SOCs can be very different (Ref. 2). The efficiency of memory testers is largely irrelevant due to the algorithmic nature of memory test and the ability to generate test stimulus and process test results in per-site hardware. The test list for memories consists of a small number of tests that have long execution times, so relatively little time is spent setting up the tester compared with the actual test time. Non-memory devices, conversely, have test lists that can be thousands of tests long, and each test may require only a few milliseconds to perform.

Table 1. Memory vs. non-memory devices

	1-GBIT DRAM	NON-MEMORY DEVICE
Number of active pins	45	<16 to >300
Incorporates BIST/DFT	No	Yes
Mixed signal	No	Yes
Single device test time	~120 s	1 to 10 s
Total production volumes	10 million to 100 million	100,000 to 10 million

Bottlenecks in the tester architecture become more and more noticeable as the number of sites increases. Every element of the tester design must be optimized for multisite efficiency. The efficiency of DC tests depends upon the ability to quickly sequence these tests under pattern control, eliminating any serial programming of tester hardware. The efficiency of mixed-signal tests depend upon the ability to move and analyze captured data quickly while testing continues in the foreground. The efficiency of many mixed-signal and digital tests depend upon the ability of the tester to independently synchronize (or match) on each site in parallel, otherwise these tests must be done serially. In other words, the tester must be designed from the ground up with a fully parallel architecture.

Figure 1, adapted from Ref. 2, shows that a tester must be more than 75% efficient to provide any real benefit beyond quad site. To be cost-effective beyond eight sites, a tester must be more than 90% efficient. Only a parallel architecture tester will be able to achieve this level of efficiency in production.

How much can a handler handle?

A crucial element of the test cell is the device handler. Pick-and-place handlers (P&P handlers) that can handle a large number of package types and a wide range of device pin counts are often used for non-memory devices. These handlers can be easily changed from one package style to another, and many support testing at ambient, cold, and hot temperatures. Inside the handler, the device goes through four basic stages:

- waiting to be tested in an input tray;
- being loaded into a carrier in the handler and brought to the correct temperature for testing;
- placed into the test socket, tested, and then placed back into the carrier; and
- sorted, where good devices and bad devices are placed into separate output trays.

P&P handlers are able to perform all four of these processes in parallel. The handler takes into account anticipated thermal soak times and presumed test times to determine how many devices to queue in the soak chamber and how many devices to sort in parallel. Like the tester, the handler represents a reasonable trade-off between throughput and expense.

Two main factors determine the throughput of a handler:

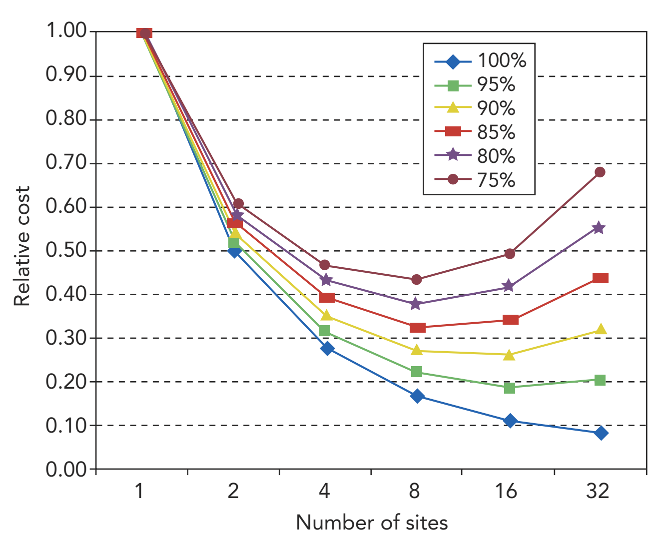


FIGURE 1. High efficiency is crucial to low cost of test. A tester must be more than 75% efficient to provide any real benefit beyond quad site. To be cost-effective beyond eight sites, a tester must be more than 90% efficient.

- *Index time,* the time required to remove tested devices from the test sockets and install fresh, untested devices. For P&P handlers, index times range from 0.4 to 0.8 s. Index time must be added to the test time of the device when calculating throughput. On some handlers, index times increase with the number of parallel sites.
- *Maximum throughput,* the maximum number of devices that the P&P handler can process in a given time period, if the actual test time is zero. The maximum throughput gives an indication of how many devices can be accommodated in the thermal soak chamber and how quickly devices can be sorted after testing is completed. Current handlers offer throughput of 5000 to 8000 UPH.

Unfortunately, the index time and the maximum throughput for most handlers differ depending on factors such as the number of parallel test sites, the size and type of the device package, and the dimensions of the device trays. Test temperature also can have a marked effect on the throughput.

Handler manufacturers will generally provide throughput curves specific to the handler model and change kit for each device type to help customers calculate expected performance. These curves represent the peak performance of the handler under ideal conditions. On a real production floor, variations in package dimensions and misalignments in carrier trays result in handler jams. Usually, an operator quickly clears these jams with a few keystrokes on the handler control panel, but while the jam condition exists, no material moves through the handler. Also, if the jam occurs in the thermal chamber or in the mechanism that presents the devices to the test sockets, the operator may need to open the handler

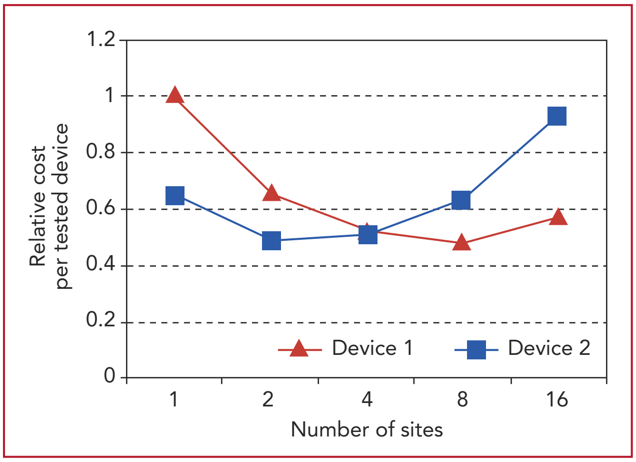


FIGURE 2. Device 1, a wireless base-band device with embedded memory, shows steadily decreasing cost of test up to an octal site implementation, but device 2, a similar device but without embedded memory and produced in lower volumes, is 30% more expensive to test at octal site than at dual site.

FIGURE 3. Lot size can have an effect on cost of test. Here, increasing lot size from 1000 to 10,000 cuts test cost 20%.

to clear the jammed devices. Handler jams are specified using two parameters:

- *Jam rate*, the average number of devices processed between handler jams. For P&P handlers, jam rates will range from 1 in 10,000 to nearly 1 in 5000. How tightly device package dimensions are maintained can affect the jam rate, as can the weight of the device, because heavier devices are less likely to be mishandled. Test temperature also has an effect, with cold temperature testing tending to have the highest jam rates.
- *Mean time to assist (MTTA)*, the amount of time required to clear a jam. Most of the time, a quick key press takes care of the jam in less than a minute, but a few jams require the operator to open the handler or break the setup and can bring down a test cell for as long as an hour. Also, the MTTA assumes that an operator is immediately available to service the test cell, instead of doing other work. For an operator working a few test cells, a reasonable MTTA is 2 to 5 min.

For multisite testing, it is crucial to remember that the jam rate is related purely to the number of devices being handled. Therefore, the selection of a handler with the lowest possible jam rate is critical to maximizing throughput. Also, the constraints will be very different for wafer probe test where throughput can be much higher and jams are not an issue.

Testing device lots

Testing ICs is a batch process. A batch, or "lot," of devices is loaded into a handler, tested, and unloaded. Then, a fresh lot is loaded, and so on. While the loading and unloading takes place, the test cell is idle.

When a lot completes, an operator summarizes the test results, unloads and labels the trays of good and bad devices, and loads fresh material into the handler. The amount of time needed for this end-of-lot (EOL) processing is almost independent of lot size but will vary depending on the level of automation. It also depends on the number of test cells each operator covers. If the operator is doing something else when a lot completes, a test cell will stand idle until loaded with fresh material. Informal manufacturer surveys indicate that a reasonable estimate for EOL processing is 5 to 10 min, mainly depending upon the number of test cells an operator manages.

The impact of this idle time on test cost is a function of the size of the lot and the amount of time required for EOL processing. The larger the lot, the longer it will take to run through the test cell, meaning that the test cell is idled less frequently and therefore more efficient. If efficiency were the only thing driving lot size, then large lots would be the best choice. Unfortunately, lot size depends on factors that often push manufacturers to make lots smaller, not larger. Customers want to keep work-in-progress inventories low and are unwilling to accept large lots, and semiconductor manufacturers are reticent to build large quantities and hold them in finished-goods inventory. In general, lot sizes are usually between 1000 and 10,000 devices. At the beginning of a production run, lots tend to be smaller, increasing in size as yields improve.

Consider a case where the throughput of a quad-site solution is 8000 devices per hour. A 2000-device lot could be tested in 15 min. If EOL processing takes an additional 10 min, during which the test cell is idle, then the test cell is idle 40% of the time, driving up the real cost of test dramatically. In contrast, if a single-site solution is implemented, testing the same 2000-unit lot may take 120 min. In this case, with the same 10-min EOL processing time, the test cell is idle only 8% of the time. The faster the tester, the more important it will be to ensure that idle time during lot processing is minimized.

Your test cost may vary

The challenge is to understand all of these effects and determine what type of setup will be the most the most cost-effective. Two specific cases help tie the effects together:

- Device 1 is a wireless base-band device with a big embedded memory. It has 80 active pins, DACs, ADCs, and multiple processor cores. Because of the embedded memory, the test time is extremely long at 15 s. Demand for this device is high, and the expected production rate is approximately 1 million devices per month for the next year. Lot sizes are 5000 devices.
- Device 2 is a wireless-networking base-band device with the same pin count. It

also has DACs, ADCs, and processor cores, but no embedded memory. Without the memory, and because of some effective DFT, test time is a blistering 5 s. Production is ramping up, and 10,000 devices will be shipped per month for the next year. Volumes are moderate—lot size is 1000 devices.

Our fictional test engineer has a tester that can be configured to test any number of sites from 1 to 16, and the multisite efficiency is a respectable 95%. She has selected a P&P handler with an index time of 0.5 s and a maximum throughput of 7000 devices/hr for quad, octal, and hex configurations. For dual site, this handler has a throughput of 3500 devices/hr. For single site, throughput is 1750. The handler jam rate is 1 in 5000, and MTTA is 2 min.

A model that includes all of these factors provides estimates of the cost of test for these two devices (**Figure 2**). Even though the devices are similar in many respects, the test time and production rates have a critical effect on the cost of test. While device 1 shows a steadily decreasing cost of test up to an octal site implementation, device 2 is 30% more expensive to test at octal site than at dual site.

The same model can be used to understand the potential impact of making changes to the production testing. For example, the test engineer could examine the effect of making the lots larger for device 2 (**Figure 3**). If she can increase the lot size to 10,000, she can cut the cost of test almost 20%—a much better result than she would obtain by adding sites.

Minimizing the cost of test for complex non-memory devices requires more thought than just doubling the number of devices tested in parallel. Even though memory devices have shown that massive multisite is a valuable strategy to minimize cost of test, non-memory devices present a different challenge to test cell throughput. **Table 2** includes some of the major factors that can influence the economics of multisite solutions.

Table 2. Factors affecting test cost

Massive multisite may *reduce* cost of test if...

- Tester has a parallel architecture with multisite efficiency >90%
- Total production volume exceeds 1 million
- Test time is greater than 10 s (usually infers device includes embedded memory)
- UPH of handler does not limit throughput
- Jam rate is low (>1:10,000)
- Lot size is large (>5000)
- Device pin count is small, or reduced pin-count testing is used

Massive multisite may *increase* cost of test if...

- Tester has bottlenecks that limit multisite efficiency to <90%
- Total production volumes are less than 1 million
- Test time is less than 10 s
- UPH of handler limits the throughput
- Handler assist rate is <1:5000
- Lot size is small (<2000)
- Device pin count is large

The one constant in semiconductor test is change. Tester and handler manufacturers are constantly refining technology and working with device manufacturers to explore new technologies to break these barriers. Other types of handlers, including strip-test handlers and matrix handlers, have been developed to handle devices in groups rather than individually. Also, P&P handlers are constantly improving to offer higher throughputs, lower jam rates, and advanced features to minimize MTTA. As these technologies come on line, the economics of multisite testing will evolve, and reductions in cost of test will continue. T&MW

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2. LaBonte, Harold, "It's all about the Architecture," *The Final Test Report*, Vol. 16, No. 2, February 2005, www.finaltestreport.com.

Greg Smith *was a consultant specializing in semiconductor ATE and handling systems when he wrote this article. He has now joined Teradyne in a technical marketing role. He previously held leadership roles in product development, marketing, and applications at LTX.*

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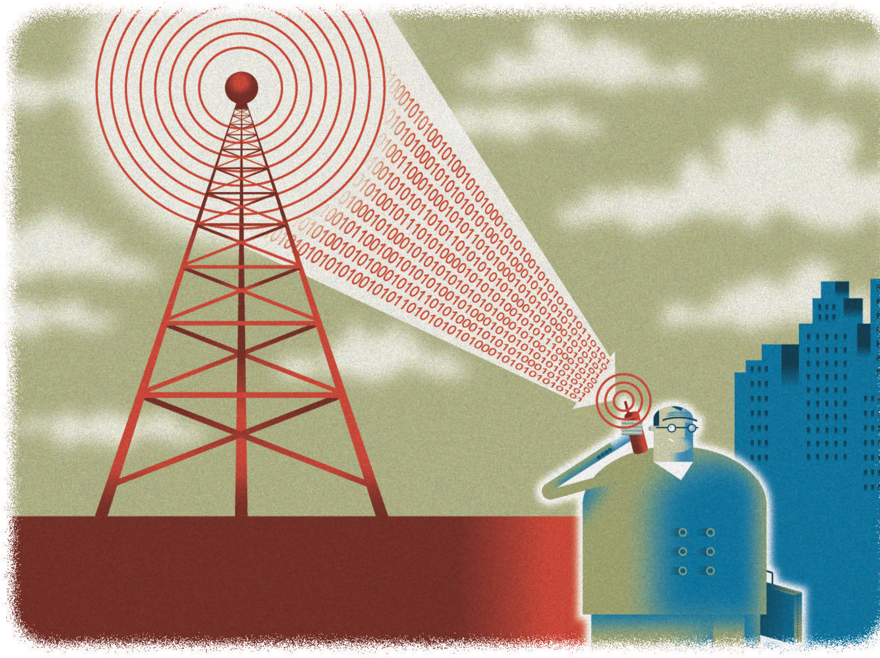
Test methodologies must evolve as GSM and WCDMA combine with High-Speed Downlink Packet Access.



HSDPA TESTING

DR. SALIM MANJI, SPIRENT COMMUNICATIONS

UMTS wireless network operators have recently taken a giant step forward by deploying WCDMA service alongside existing GSM services. This deployment was not a minor undertaking, as GSM and WCDMA are based on two very different technological foundations. Now, network operators are facing even greater challenges as they prepare to implement High-Speed Downlink Packet Access (HSDPA), a data-transmission technology that has evolved from WCDMA.

Like any CDMA technology, WCDMA is a spread-spectrum technology that introduces a new domain—the code domain—in which orthogonal spreading codes at the physical layer differentiate channels. Because the physical layers are different, the effects of air-interface phenomena ripple up the WCDMA and GSM protocol stacks differently.

The WCDMA service now offered is known as Release 99 service, named after the currently deployed version of the 3rd Generation Partnership Project (3GPP) UMTS/WCDMA technical specification. Network operators will soon be taking the next step by implementing HSDPA, a new service that will coexist with Release 99 and, in most cases, share space with older networks. Although early HSDPA deployments are likely to be on a par with current broadband speeds, HSDPA offers theoretical data rates of up to 14 Mbps.

Test engineers have just finished bridging the chasm between GSM and Release 99, and some are tempted to treat HSDPA as just a "faster Release 99." There are key differences between the two, though, and they are significant enough to require a closer look. As the name implies, HSDPA is meant for downlink data traffic only, and it offers several enhancements for handling this traffic. To ensure the HSDPA technology works properly in the field and is well received by users, the industry will need to devise new test methods that are designed specifically for data-centric transmissions.

HSDPA vs. existing technologies

Release 99 is largely built on the traditional CDMA principle of separating users in the code domain. With the Dedicated Physical Channel (DPCH) technology in Release 99,

network operators are able to manage the user population in a cell. The use of fast power control ensures equality among users, which allows for maximum cell capacity. Mobility can be managed effectively through the use of soft handovers.

This configuration works well for moderate data rates, but to support high-data-rate users, a provider must allocate a large portion of the code space, which diminishes the available cell capacity for other users. Since data traffic is often bursty, physical-layer resources may not be in use all the time. Quick reallocation of resources to support the "instantaneous" demands of the users in a cell is difficult to achieve in Release 99.

In contrast, HSDPA was designed with data in mind. The technology uses the benefits of the CDMA air interface while also optimizing network operation for data users. The network allocates one "fat pipe" for high-speed data, and the remaining cell resources can still be used for voice and low-rate data traffic. The network operator chooses how to allocate resources among high-speed data and all other users.

HSDPA's "fat pipe" is known as the High-Speed Downlink Shared Channel (HS-DSCH), and it may be shared among multiple users. The HS-DSCH is relatively static in terms of CDMA resources. For example, the spreading factor (the factor by which conversion to the code domain "spreads" the signal spectrum), maximum number of code channels, and code powers are generally constant, unlike in Release 99. Therefore, the network has a fixed resource to work with and can efficiently serve the high-speed data user population. Users with the best chance of getting higher-rate data are assigned more of the shared resource, based on proximity to the cell, lack of other users in the area, and signal strength.

HSDPA offers several ways to optimize resource allocation, including Adaptive Coding and Modulation (ACM), Medium Access Control high-speed (MAC-hs) scheduling, and the Hybrid Automatic Repeat Request (HARQ).

Fast ACM

Fast ACM replaces the Release 99 DPCH's reliance on "fast" or inner-loop power control as a solution to the "near-far" problem. If a Release 99 device is close to a Node B base station, the Node B base station can adjust power so as to equally share resources among subscribers. In contrast, in HSDPA the Node B base station implements ACM in such a way that it adjusts the data rate, and not the associated power, to make the best use of network resources.

The data rate is adjusted by two methods. The first is adaptive modulation. An HSDPA signal can employ quadrature phase-shift-keying (QPSK) modulation, as in Release 99, or it may employ the more efficient 16QAM (quadrature amplitude modulation with 16 target symbols), but only if the receiver provides sufficiently good reception, because 16QAM signals are more difficult to demodulate than QPSK signals. A receiver can demodulate a QPSK symbol as long as its phase can be determined within 90°, while demodulation of a 16QAM signal requires a little more processing (**Figure 1**). In fact, 16QAM phase detection must be better than QPSK phase detection by a factor of three for proper demodulation; a 16QAM symbol may be only 26.6° out of phase from another symbol. And 16QAM poses an additional challenge: Amplitude detection is unnecessary in QPSK reception, but it is a key part of QAM demodulation.

HSDPA's second data-rate adjustment method is adaptive coding. To correct errors on the fly, WCDMA uses redundancy coding, which sacrifices bit rates to gain error-correction capability. If the mobile unit's reception will support it, the data rate can be adjusted by optimizing the coding rate and the number of code channels for a user.

MAC-hs scheduling and HARQ

In Release 99 networks, a Radio Network Controller (RNC) handles scheduling. This approach works well enough for voice networks, but for efficient data transmission, HSDPA uses an alternative approach. Since the Node B base station is always the first link in the chain from phone to network, the Node B itself handles scheduling in HSDPA, taking advantage of the fact that bursty data scheduled for a number of users will most likely not be transmitted at the same time. Data traffic targeted for a number of users can be statistically multiplexed. By moving the MAC-hs into the Node B, HSDPA traffic can be scheduled at a time resolution of 2 ms, much tighter than in Release 99.

The MAC-hs handles not only the scheduling of transmitted data, but also the scheduling of HARQ retransmissions. While the ACM process performs some error correction, the HARQ function is responsible for recovering from errors where channel coding alone is not sufficient. In other ARQ processes, the receiver throws an erroneous packet away and sends a NACK message to the trans-

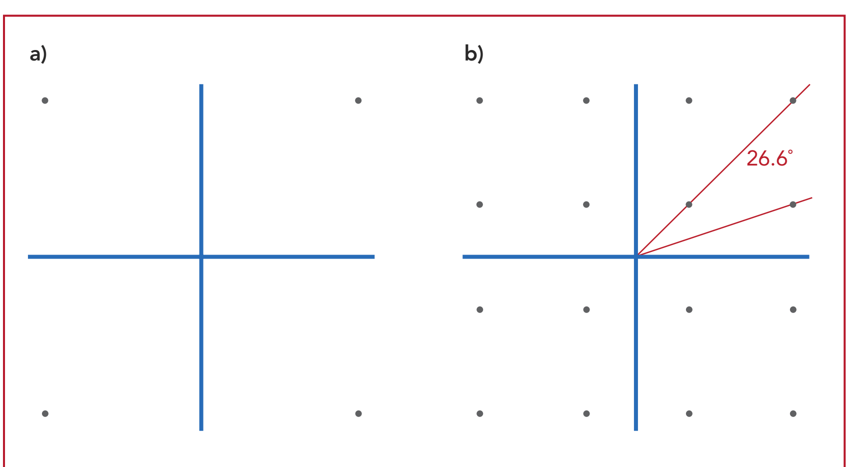


FIGURE 1. Constellation diagrams indicate the relative complexity of 16QAM vs. QPSK modulation schemes. (a) A QPSK symbol can be demodulated as long as its phase can be determined to within 90°. (b) In contrast, a 16QAM symbol can be no more than 26.6° out of phase from another symbol.

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mitter, which retransmits the packet. In the HARQ process, the receiver saves, rather than discards, an erroneous packet, making use of its residual information in combination with the retransmitted version in a seemingly complex process that actually improves performance in wireless applications, where impairments are a fact of life.

Isn't 3GPP testing enough?

3GPP offers a set of test specifications designed for testing UMTS mobile devices, including HSDPA devices. These tests ensure that a mobile device meets a set of minimum acceptable standards. Network operators have to balance operational costs in order to offer attractive pricing, and the 3GPP will make sure that they have that chance. What the 3GPP does not do is perform design verification or competitive analysis, or predict loads on network resources.

Consequently, a large body of important testing is not defined by the 3GPP. To please wireless consumers who use ever-increasing amounts of bandwidth to receive and transmit data, network operators are relying on engineers in labs all over the world who are pursuing new, effective ways to use performance testing to test critical cellular characteristics.

Most performance testing uses 3GPP-defined standard tests as a starting point. For example, the 3GPP defines a test with hard pass/fail limits to verify that HS-DSCH reception by a mobile device meets a minimum set of throughput requirements. As defined, this test includes a number of variations based on the stated capabilities of the mobile device. It does not characterize the device, but it does provide an excellent starting point for doing so.

One portion of the 3GPP document describes a test called Single Link Performance (Ref. 1). This test procedure includes a lot of detail regarding different conditions that must be tested: multipath (signal reflection) conditions, throughput targets based on modulation schemes, and references to different sets

What about field testing?

Field tests for mobile devices must be run on a "live" network, the same air interface used by paying subscribers. This can be dangerous; a buggy phone may not only work poorly, it can also affect other subscribers. In UMTS (including HSDPA) testing, a buggy phone can "steal" network resources from paying subscribers. This can be difficult to recognize, especially when the one phone that is stealing resources is a prototype among a thousand proven designs.

HSDPA testing adds another wrinkle that can make field test difficult. Remembering that HSDPA employs a shared downlink channel, note that the technology depends on adaptive coding, where code-domain resources are allocated depending partially on resource demand. In a live test, it can be difficult to keep track of users who are competing for shared resources; if an error occurs, a mobile device that performs well can seem to have throughput problems. Unless you have complete control over the network, the best test plan can provide incorrect results.

Field tests are also not conducive to "adversarial" testing, where the network is purposely compromised to simulate a software error, faulty hardware, or some network resource constraint. It is possible to selectively alter network configurations for a particular subscriber, but these configurations can be tedious to set up, and the results of a mistake can cause problems for commercial subscribers.

Finally, engineers who test for a living understand that a test worth doing must be repeatable. Live network conditions change by the minute, and it's nearly impossible to be aware of all the changes. Lab-based testing gives an engineer complete control over all aspects of the cellular environment, including network configuration, resource availability, power, channel fading, and service availability.—*Salim Manji* of parameters. Understanding the pass/fail test requires some knowledge of multipath and the fading environment, and it requires a lot of poking around through appendixes in the specification as well as related specifications.

Once you understand the test, you can create many variations. For example, suppose you want to know how throughput rates vary with fading or noise. Or suppose you want to find out what happens if Node B isn't behaving ideally. What if the fading models defined for this test don't accurately reflect the fading conditions that the customer will experience? All of these are opportunities for performance tests.

It is impossible to define the "perfect" set of performance tests for HSDPA, which is another reason why the 3GPP doesn't define detailed performance tests. There are a seemingly infinite number of options, and these must be winnowed down to those that apply in each case. If history is any guide (and it usually is), there will be surprising variations in the performance of commercially deployed devices.

Performance testing on Release 99 handsets, for example, has shown dramatic differences among a sample set of phones, all of which passed the tests defined in the standard. These results show that consumers will have different experiences, that network operators will bear different deployment costs, and that handset manufacturers will enjoy or endure the long-term effects of brands associated with performance disparities.

Field testing may seem to be the ultimate in realistic testing. But while in-field beta testing should be done before any product is released, field tests present very real limitations (see "What about field testing?" at left); they can interfere with paying consumers, for example, and they are rarely repeatable.

End users will perform the ultimate long-term field test. Their perception of HSDPA will be the one that counts. Yet, the quality of their experience will depend on the quality of performance testing done beforehand. These "real-world testers" will be the ones who vote with their wallets and eventually decide on the futures of device makers, network operators, and HSDPA itself. T&MW

REFERENCE

1. The Single Link Performance test is described in Section 9.2.1 of 3GPP TS 34.121, "Terminal Conformance Specification, Radio Transmission and Reception (FDD)," The 3rd Generation Partnership Project, www.3gpp.org/ftp/Specs/html-info/34121.htm.

Salim Manji *is a product manager at Spirent Communications in Eatontown, NJ. He earned a PhD (2004) from Rutgers University's Wireless Information Network Laboratory (WINLAB), where his thesis concerned image transmission over high-speed cellular networks in the presence of fading. His work at Lucent's Bell Labs involved early research on such topics as MIMO over UMTS and HSDPA.*


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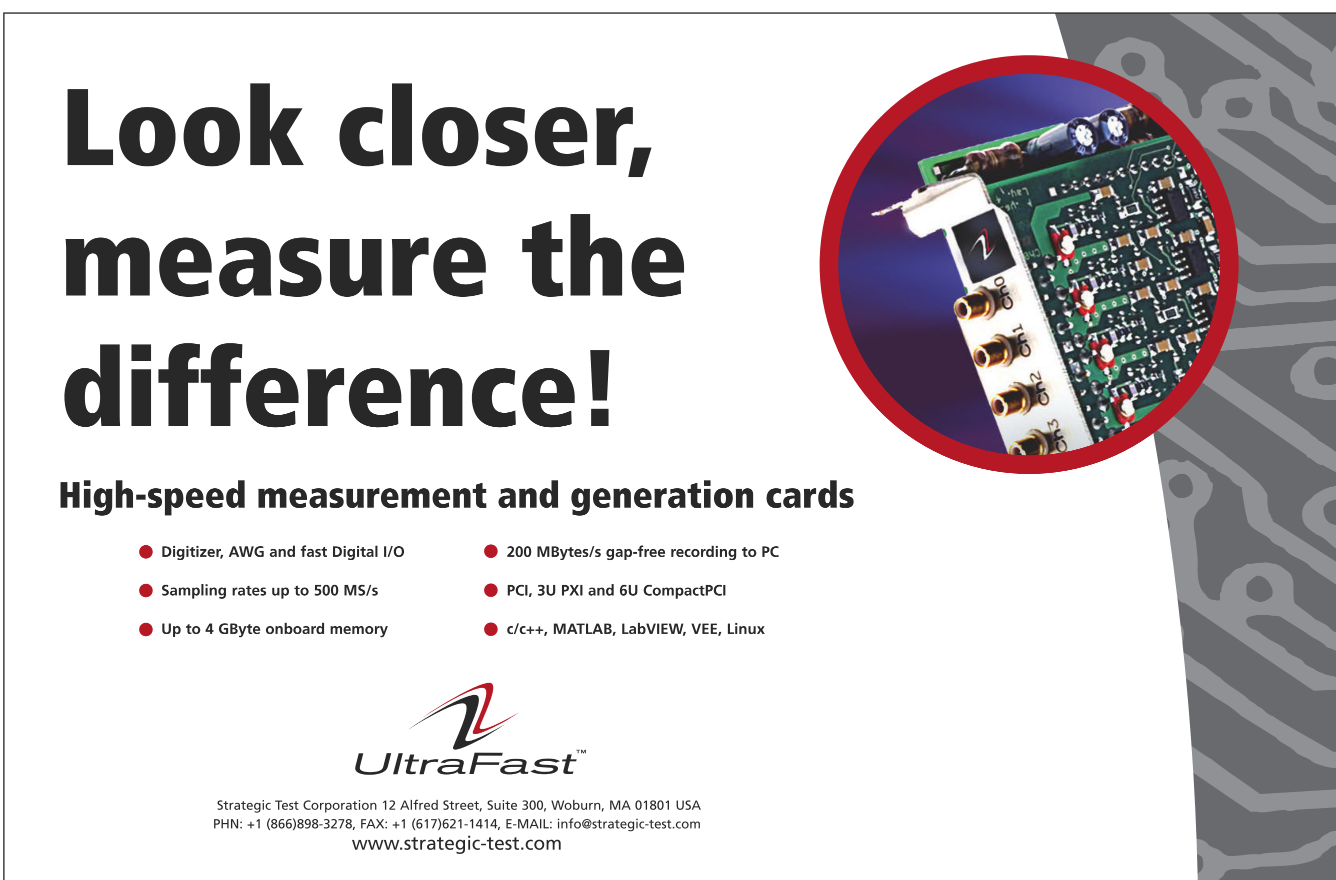
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Test & Measurement World

Automotive & Aerospace TEST REPORT

RESISTANCE TEST

Strain gages measure automotive forces

Greg Reed, Contributing Technical Editor

In 1856, Lord Kelvin observed that metallic conductors subjected to mechanical strain exhibit a change in their electrical resistance. Since that time, engineers have attempted to measure and quantify strain by converting mechanical motion into an electrical signal. In automotive applications, Ralph Shoberg, founder and president of RS Technologies, has gained a reputation for extracting precise strain measurements from a multitude of moving parts. In a recent telephone conversation, I spoke with him about strain gages and ways to apply them.

Q What components are in a typical automotive strain-gage system?
A The strain-gage system begins with the strain gages themselves. We use what are technically termed "bonded metallic foil grid resistance strain gages." These are extremely thin foil grids with an equally thin nonconductive substrate that are bonded to the component under test. The gages are usually wired together into a Wheatstone bridge circuit that typically uses strain-gage elements in multiples of four. Instrumentation excites the bridge and conditions the strain-gage output signal into meaningful engineering units. Computerized data-acquisition systems can be configured to interface with virtually hundreds of data inputs.

Q As a custom strain-gage engineering provider, what types of automotive applications does RS Technologies service?
A We have serviced a variety of applications, the majority of them involving some sort of torque or force measurement. The most common application is for driveline torque measurement, either on a rotating drive shaft or half-shaft. But essentially any component that is placed under some sort of stress during vehicle operation can be gaged and the resulting forces measured.

Q Can you provide some tips for applying strain gages?
A The most important step in engineering a strain-gage application involves a pair of decisions. The first is the selection of the proper size and type of strain gage. Included in the strain-gage selection process is selection of the correct gage factor, which is the resistance change of the gage when placed under strain. A general rule of thumb is the more deflection of the part, the lower the gage factor. And conversely, the less the deflection, the higher the gage factor.

The second important decision is the proper placement of the gages on a spot where the stress being transmitted through the component can be measured. Correct decisions about gage type and placement will largely determine the accuracy and success of the measurement.

Ralph Shoberg, founder and president of RS Technologies.

Q What are some specific challenges in mounting automotive strain-gage equipment?
A The greatest challenge is probably gaging the components without affecting their usual operation. If the strain-gage system or instrumentation impacts the weight and performance of the component, the effectiveness of the data will be limited. Thus, it is important to keep the weight of the components low and minimize or eliminate interference with the operation of the component and the vehicle.

Q How does one go about acquiring data from a strain-gage system?
A There are several approaches to data acquisition. In some cases, all that's required is a peak measurement. In other cases, a dynamic trace is required to observe the strain over a variety of loads or operating conditions. Data-acquisition systems range from simple readout instruments to high-speed, high-accuracy computerized systems. At the least, they will have the proper power supply and signal-conditioning circuitry so that the data measurement can be observed or recorded. □

For the complete interview, see the online version of this article at www.tmworld.com/auto.

INSIDE *this issue*

EDITOR'S NOTE

MEMS accelerate auto test

Greg Reed, Technical Editor

According to recent market reports, shipments of microelectromechanical systems (MEMS) are set to double over the next five years. Researchers also cite the automotive sector, with several high-volume safety products, including air

bags and tire-pressure monitoring systems, as being the primary application field for these devices.

MEMS represent the integration of mechanical elements, such as sensors, actuators, and accelerometers, with electronics on a common silicon substrate. The electronics get manufactured using standard semiconductor processes, while the mechanical parts are micromachined by etching the wafer or adding structural layers on the silicon. These systems-on-a-chip enable the development of smart products by adding perception and control to established computational microelectronics.

Test engineers must be engaged throughout the semiconductor fabrication process, the parallel micromachining processes, the implantation in specific components, and the assembly of the automotive subsystem. In practice, MEMS mimic traditional industrial age movement, positioning, regulating, pumping, filtering, and controlling actions on a microscopic level. With MEMS already well-established in air-bag deployment, bumper sensing, and tire-pressure regulation, automotive and aerospace applications for these systems abound while test personnel ensure quality and reliability at six-sigma levels. □

Contact Greg Reed at editor@aatr.net.

NEWS

NTS upgrades EMI test capabilities

NATIONAL TECHNICAL Systems has outfitted three of its facilities to incorporate 200-V/m interference testing for military and commercial avionics. New RF power amplifiers at the facilities (Plano, TX; Boxborough, MA; Fullerton, CA) can produce field levels above MIL-STD-461 and RTCA DO160 requirements. The new capability simulates high-intensity radar sweeps encountered in hostile combat areas and in commercial operations when crossing radar beams on final approach to an airport.

The multimillion dollar expansion was started in 2003 and included the installation of several walk-in 7000-ft^3 shielded rooms as well as signal generators and RF-power amplifiers with frequency outputs ranging from 10 kHz to 40 GHz. The range of equipment that can be tested include shipboard equipment, ground-based equipment, navigation and control systems, engines and power systems, airborne weapon platforms, and communication systems for aircraft, unmanned airborne vehicles, missiles, and smart munitions. The largest of the electrically shielded rooms measures 40x30x20 ft with double-wide doors for large systems or complete missiles. www.ntscorp.com. □

Canada's Defense Department selects Raytheon test bench

The Canadian Department of National Defense has selected Raytheon Canada to provide an enhanced APG-73 test bench capability for the Canadian Air Force. The contract is valued at CDN $12.4 million ($10.5 million US).

The new equipment will be installed at Raytheon Canada's Calgary facility to expand radar capability. The test bench will enable diagnostic testing of the radar, which is located in the nose of the CF-18 aircraft. It will also permit target simulation and generation, troubleshooting, technical investigations, and the provision of software and engineering support. www.raytheon.com. □

LMS software helps Chinese researchers develop jet

Design and engineering teams at the First Aircraft Institute (FAI) of AVIC-1, a leading aerospace research institute in China, have used LMS Virtual.Lab simulation software to support development of the advanced regional jet program, ARJ21. Developed to meet China's growing need for air transportation, the ARJ21 will accommodate up to 100 passengers and will be available in freight, business jet, stretch, and extended-range versions.

The research institute employed the LMS software during the design and engineering of the aircraft body and landing gear development. The simulation suite provided finite-element and preprocessing and postprocessing on components, subsystems, acoustics noise analysis, and design alternatives. www.lmsintl.com. □

Calendar

SAE World Congress
April 3–6
Detroit, MI
www.sae.org/congress

Aerospace Testing Expo
April 4–6
Hamburg, Germany
www.aerospacetesting-expo.com

Defense Standardization Program Conference
May 23–25
Arlington, VA
www.sae.org

TEST SERVICES

Tips for choosing a test lab

Thomas Rinke, Vehicle Research and Development

What factors do you need to assess when searching for a testing service provider? No matter what type of tests they perform, independent test laboratories should adhere to a set of fundamental principles in order to provide high-quality service. Here are some key factors you should consider when evaluating a prospective testing service provider.

Client selection

One of the best resources when searching for a suitable testing service provider are your own customers, who most likely have a list of preferred vendors who specialize in testing in your market segment. Ask them for the most responsive testing providers they have encountered in recent years. You should also seek referrals from original equipment manufacturers (OEMs) and other tier suppliers. Manufacturers often use a third-party test provider to conduct their validation testing.

Find out how responsive the provider is to customer inquiries. Ask for references and follow through on contacting them.

Service

Does the testing provider offer the range of services you need? Depending on your project timing, you may need a provider who offers round-the-clock testing services. Ask if the provider offers continuous testing throughout all 24 hours of the day, including weekends and holidays. Also, ask if the lab is staffed at all times of the day or if it is automated to conduct the tests.

Consider the final results of the lab or test procedures. Will you receive a summary of the findings? Is raw data available? Can you obtain electronic and hard-copy results for your test? Will the findings summarize the results with easy-to-read graphics?

Equipment

Having the proper test equipment in place is a hallmark of a quality testing provider. Be sure to go on a tour of the testing facilities. Inspect the equipment and general presentation of the facility. Is the environment clean? Do you sense that safety is important at the facility? Ask how the test is set up with the equipment for all nonstandard tests.

Allow the testing provider ample time to configure the proper equipment to conduct your tests. Most test providers specialize in particular types of procedures. If you are looking to run transmission tests, for instance, be sure the facility you are evaluating is equipped to handle such tests. Often, test providers can refer or subcontract clients to other providers who specialize in a particular type of test or laboratory service.

Over 45 kW of heat penetrate down on the top of a vehicle during an infrared heating test within a drive test chamber.

Facilities

During that critical facility tour, find out where customer material is stored. Does the staff ensure confidentiality for customer material and prototype components? Is there ample warehousing space for extra storage requirements? Will your material remain on site at the company's lab, or will it be sent out to a secondary shop? Does the facil-

Tips • from page 45

ity have security measures that satisfy your requirements?

Quality accreditation

Make sure that the testing provider has been accredited to offer testing services. For standard and nonstandard testing, there are various testing accreditation bodies and consortiums who verify that certain quality issues are addressed by the provider.

ISO/IEC is acknowledged as an international benchmark for approving the competence of the testing and calibration laboratories that play a role in trade, in product development and manufacturing, and in protection of the consumer. Make sure your testing service provider is accredited to the latest edition of any relevant ISO/IEC standards. Nonprofit, public agencies such as the American Association for Laboratory Accreditation (A2LA) offer proficiency testing certification. A2LA is dedicated to the recognition of competent testing and calibration laboratories, inspection bodies, proficiency testing providers, and reference material producers.

Personnel

When interviewing providers, ask to meet the customer service personnel, the test technicians, and the project manager in charge. Is an engineer on staff to assist in configuration and setup of all tests? All of these individuals should be available to you when evaluating a test service provider. Just like the equipment and the facilities, the personnel are a key component to finding a quality provider.

Final questions

Be sure to ask any other questions that come to mind to ensure the test service provider can handle your project. How long has the testing facility been in business? Is the testing service able to accept new clients? Can the firm handle a large client request? How much notice is needed to begin testing?

Because it is their business to conduct tests for customers, independent test laboratories have made substantial investments in the required equipment and expertise. Finding the right test laboratory for nearly any kind of test, including electrical, mechanical, environmental, powertrain, and physical tests, can be a rewarding experience if you do a little homework before signing a contract. □

Thomas Rinke is the general manager of Vehicle Research and Development in Almont, MI. He holds a BSME from the University of Michigan. trinke@vrdtest.com.

PRODUCTS

ECU electrical/optical tester

Goepel Electronic teams its magicCAR electrical test system with the TOM AutomotiveLine optical inspection system to perform both functional test of electronic control units (ECUs) and optical inspection of controlled modules, such as pointer instruments, LEDs, and displays. A universal test environment for vehicle ECUs, magicCAR generates simulated signals and communication interfaces (CAN, LIN, and K-Line) for analysis through an automobile control unit. *Goepel Electronics, www.goepel.com.*

Automated bed-of-nails tester

Strategy.sl integrates in-circuit, functional, and visual test functions on a fully automated SMEMA (Surface Mount Equipment Manufacturer Association) standard conveyor for loading and unloading of boards under test, allowing integration into an automated production line or a stand-alone test island. You can develop, debug, and run test programs on any system in the Strategy line and move them to the automated Strategy.sl when production ramps up. *Seica, www.seica.com.*

Signal-conditioner board

Small enough to be built into a load cell, extensometer, or pressure sensor, the CellMite M4326A digital signal-conditioner board with TEDS-Tag Auto-ID automatically selects the correct sensor calibration and analog output scaling for the connected transducer. CellMite simultaneously generates a serial output for connection to a PC, as well as a ±10-V analog output. The tiny board provides 24-bit internal resolution, internal temperature compensation, a sampling rate of 60 samples/s, and multidrop RS-232 communication. *Electro Standards Laboratories, www.electrostandards.com.*

RS-422/485 universal PCI card

Built to work with both 3.3-V and 5-V PCI bus systems, the PCI-1622CU PCI card supplies eight RS-422/485 ports for communication with up to 32 devices. In RS-485 half-duplex mode, only two wires are needed to transmit and receive data. The PCI-1622CU automatically senses the direction of the data flow and switches the transmission direction. No handshaking is necessary, and control is completely transparent to the user. The card's surge protection shields the host system from abrupt high voltages up to 2500 VDC. *Advantech, Industrial Automation Group, www.advantech.com.*

Test & Measurement World

Machine-Vision & Inspection
TEST REPORT

MANAGEMENT

Vision company looks to the future

Steve Scheiber, Contributing Technical Editor

In November 2005, RVSI Inspection, a developer of systems used in wafer and package inspection, appointed Kevin Maddy as its new president. RVSI Inspection was formed in the spring of 2005, when Ancora Management purchased the assets of the Semiconductor Equipment Group from Robotic Vision Systems Inc. (RVSI), a division of Acuity CiMatrix.

Maddy comes to RVSI Inspection not from within the electronics industry, but from major corporations such as Ford Motor Co. and United Technologies. To date, he has focused primarily on operational issues, including opening a spares depot in Asia to better support customers there and developing enhancements to improve product quality, reliability, and performance.

"My background is centered in the automotive and aerospace industries, where I managed manufacturing plants," said Maddy. "I understand the rigors of both low- and high-volume production. The situation is simply that our customers expect a quality product delivered on time at a competitive price—with no excuses. I intend to drive RVSI in that direction using lean manufacturing techniques and integrated product development. We will also listen carefully to our customers and work with them to meet their needs."

Kevin Maddy, president of RVSI Inspection.

Maddy described "lean manufacturing" this way: "Lean manufacturing focuses on eliminating process waste, thereby improving customer satisfaction and operating margins. Also known as the 'Toyota Production System,' it has been around for nearly 80 years, yet only 10% of industry has adopted it. I have well over a decade of experience implementing it."

Changing business metrics

Maddy continued, saying, "Quite frankly, to dramatically change business metrics, you have to dramatically change your production processes and support activities. These changes must include the way the organization thinks and acts throughout the entire value stream.

"Any business process consists of 95% waste, including overproduction, excessive inventory, excessive transportation, overprocessing, unnecessary motion, workers waiting, and quality problems. Waste adds to cost, lead times, and frustration, and reduces product quality. Customers are not willing to pay for it.

"Lean manufacturing also demands improving communications within the company. For example, every employee should know the status of key operating parameters—especially cash, profitability, and customer satisfaction. That knowledge helps everyone focus on the tasks at hand.

"Another way to improve communication is to locate production leadership, quality, and engineering on the shop floor together with the machine operator. Such proximity permits solving problems faster and more effectively.

"Employees become excited about getting involved and giving their input. They are more satisfied with their work and have a better attitude about themselves, their co-workers, and the company. I expect that with these techniques, we will achieve a repeatable 80% reduction in lead times within six months while our business grows and inventory shrinks."

When asked about his perceptions of RVSI Inspection, Maddy remarked, "I am impressed with the quality and capability of our company's products and their ability to meet customers' needs, and the people are skilled and know what needs to be done. The business outlook is excellent. We increased production rates by 100% from Q3 to Q4 last year, and we plan another 150% increase in 2006.

"The market is strong and I am very pleased by the confidence in us shown by our customers. We merely have to flawlessly deliver on our promises and commitments." □

INSIDE *this issue*

EDITOR'S NOTE

Draper winners invented an industry

Steve Scheiber, Technical Editor

Genuine engineering breakthroughs don't happen very often. When they do, they deserve to be recognized.

The National Academy of Engineering recently awarded the 2006 Charles S. Draper Award to George Smith and Willard Boyle. According to the NAE Website (www.nae.edu), the annual award goes to "an engineer whose accomplishment has significantly impacted society by improving the quality of life, providing the ability to live freely and comfortably, and/or permitting the access to information." Smith and Boyle own the basic patent for the charge-coupled device (CCD) that they developed at Bell Laboratories in 1970. The two men will split the $500,000 prize.

CCDs represent the basic technology that spawned the digital imaging industry. CCDs replaced Vidicon tubes as camera sensors, so imaging was no longer restricted to large cameras whose timing was defined by the designers of conventional television. The new approach permitted adjusting image-acquisition resolution and timing to reflect the target application.

In addition to his work on CCDs, Dr. Smith was involved in a variety of investigations on junction lasers, semiconducting ferroelectrics, electroluminescence, and transition-metal oxides. Dr. Boyle was the first to use infrared spectroscopy to measure donor and cyclotron energy levels and developed the first continuously pumped ruby laser. □

Contact Steve Scheiber at sscheiber@aol.com.

NEWS

Inspection systems add Dalsa cameras

NEXT INSTRUMENT, a Korean supplier of flat-panel display inspection equipment, has announced that it will incorporate Dalsa cameras in its inspection systems that search for defects on flat-panel televisions, notebook PCs, and LCD monitors during manufacturing. Under terms of contracts totaling CDN $1.3 million, Dalsa will provide its latest generation of electronic cameras, which are designed to image at very high speeds under low light conditions. www.dalsa.com. □

Siemens acquires vision pioneer

SIEMENS REPORTS that it has acquired the assets of RVSI Acuity CiMatrix, the developer of the 2-D Data Matrix code. The acquisition "will allow Siemens to expand its factory automation vision sensor portfolio," according to Aubert Martin, president and CEO of Siemens Energy & Automation. Another division of RVSI was earlier sold to Ancora Management and became RVSI Inspection (see p. 49). www.usa.siemens.com. □

Rudolph and August proposed merger advances

RUDOLPH TECHNOLOGIES, a manufacturer of process-control metrology and defect-inspection systems used by semiconductor device manufacturers, and August Technology, a supplier of inspection and defect-analysis solutions for the microelectronic industries, have announced that the Securities and Exchange Commission has declared effective the S-4 registration statement concerning the agreement and plan of merger between them.

The joint proxy statement/prospectus that is contained in the registration statement will be mailed to Rudolph stockholders and August Technology shareholders of record as of January 5, 2006. The companies will then hold separate special meetings of their shareholders on February 15 to hold votes on the proposed merger.

On June 28, 2005, Rudolph signed a definitive merger agreement with August Technology, which was unanimously approved by the board of directors of both companies. The proposed merger is expected to close in Q1 2006. www.augusttech.com; www.rudolphtech.com. □

Firms collaborate on DPM readers

Codeveloped by Cognex and Hand Held Products, the DataMan 7500 series handheld direct part mark (DPM) readers are designed for manufacturers implementing part traceability programs in various industries. The series combines Cognex's IDMax code-reading software with an UltraLight illumination technology to read codes regardless of marking method, part material, shape, or surface texture. The product is available in both corded and cordless models.

"Collaborating with Hand Held Products, the leader in image-based auto ID, allows us to deliver industry-leading Cognex DPM reading technology in the rugged, ergonomic form factors that industry demands," said Justin Testa, Cognex Senior VP, ID Products. "Going forward, we will work together with Hand Held Products to deliver wireless and mobile solutions for DPM ID." www.cognex.com. □


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STANDARDS

Camera Link and GigE improve image speeds

Steve Scheiber, Contributing Technical Editor

As cameras used for inspection must produce ever-higher-quality images and as image-processing speeds increase dramatically, data transmission rates have remained a bottleneck for vision systems. Communication standards designed for more leisurely data environments have not proved adequate for handling the demands of inspection applications. To address this situation, two vision standards have emerged to provide faster, more reliable data transmission—Camera Link and GigE Vision

Camera Link comes of age

Camera Link grew out of the need to standardize interconnections—especially cables—between cameras and frame grabbers. Steve Kinney, who is a product manager for JAI Pulnix and a Camera Link committee chair, put it this way: "Camera Link defines a complete interface that provides a path for data transfer, camera timing, serial communications, and real-time signaling to the camera."

The Camera Link standard was developed by camera manufacturers themselves, specifically for connecting cameras to frame grabbers. Kinney explained, "We didn't try to adapt existing standards like USB and FireWire that had been created for consumer applications."

The standard is based on an implementation of technology from National Semiconductor that dramatically reduces the number of conductors in the cable. Camera Link uses the same standard connector for both frame grabber and camera, regardless of the (conforming) manufacturer.

Before Camera Link, industrial cameras had already advanced from analog to analog-progressive, to 8-to-10-bit (monochrome) imaging. Connecting cameras to frame grabbers involved a host of proprietary protocols and connectors, along with random pinouts, rather than a single standard. The cameras might feature a 31-pin miniature connector, while the frame grabber might use a 100-pin SCSI. Cables were unique to each brand of camera and each brand of frame grabber. A cable designed to connect a Coreco frame grabber to a Pulnix camera, for example, wouldn't work with a frame grabber from another manufacturer. Low volumes and the plethora of cable architectures meant that cables could cost $500 or more apiece.

The industry's transition to 24-to-30-bit color cameras aggravated the situation. Adapting existing techniques would have required 90-pin cables that could easily cost $1000 each. So, a group of 12 industry experts met in 1998 to find an alternative.

National Semiconductor had developed a chip that permitted passing RGB video information across a ribbon cable, using a differential clock to serialize 28 bits (24 data bits and 4 bits for camera timing), transmitting them across four parallel data lines and a clock line, converting back to the original 28 bits at the other end (**Figure 1**). This configuration supports data transfers up to 1.6 Gbps at 66 MHz. Adding a second connector provides two more 24-bit video channels and permits medium (two channels) or full (three channels) configurations and transmissions up to 4.7 Gbps at 66 MHz.

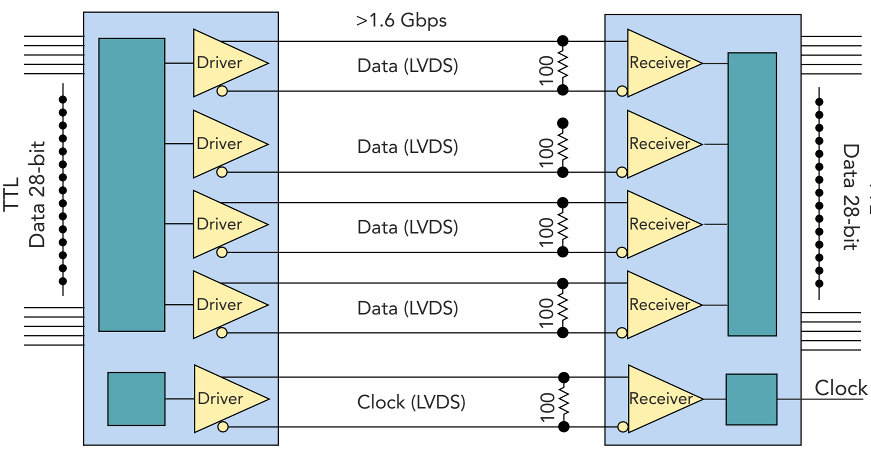


Fig. 1 A differential clock serializes 28 bits (24 data bits and 4 bits for camera timing), transmits them across four parallel data lines and a clock line, and converts them back to the original 28 bits at the other end. Courtesy of JAI Pulnix.

A frame grabber that includes both connectors will support either one full-configuration camera or two simultaneous cameras in a base configuration (**Figure 2**). In the latter case, 4 bits from the third video channel provide control for the second camera. The two-camera approach will address situations that require inspection from two angles at the same time. And although the standard limits transmission to 10 m between camera and frame grabber, the addition of repeaters can extend that distance, and a fiber-optic cable permits distances as long as 1 km.

Kinney contends that Camera Link remains the best way to build the highest-quality cameras with the fewest parts. "Camera Link provides an interconnection that is independent of image resolution, video format, and frame rate," he said. "Camera Link offers real-time asynchronous reset and camera signaling directly over the interface. That capability, along with high bandwidth, gives Camera Link distinct advantages compared to the other standards. FireWire and USB make no provision for direct real-time data transfer, signaling, or camera control."

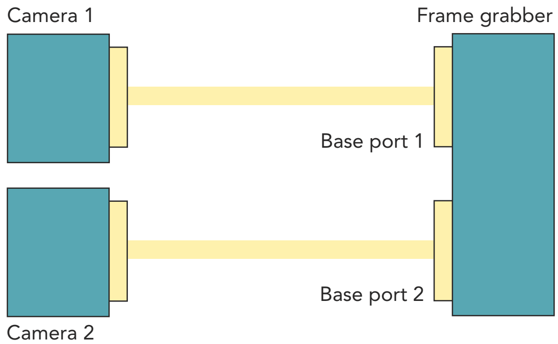


Fig. 2 The "double-base configuration" allows a single frame grabber to support two base configuration connections. Courtesy of JAI Pulnix.

In addition, designing a universal cable around a 3M MDR 26 connector dramatically reduces costs. A 2-m Camera Link standardized cable usually costs less than $100.

Standard progress

The original Camera Link standard provided a straightforward solution that has not changed much. Initially, communication was done through a manufacturer-supplied .dll file that provided such basic commands as "open port" and "write to port." Version 1.1 merely cleaned up some verbiage, added a communications link to the controlling PC, and allowed for error handling. The improved communication link provided a supervisory layer as a means to control several different Camera Link communications ports in a system with multiple frame grabbers installed.

In 2005, a miniature version of the original connector was proposed to the Camera Link Committee. With some minor changes to the specification, the committee approved the new connector, and it has begun to appear on many manufacturers' products, including a new line of cameras by Sony.

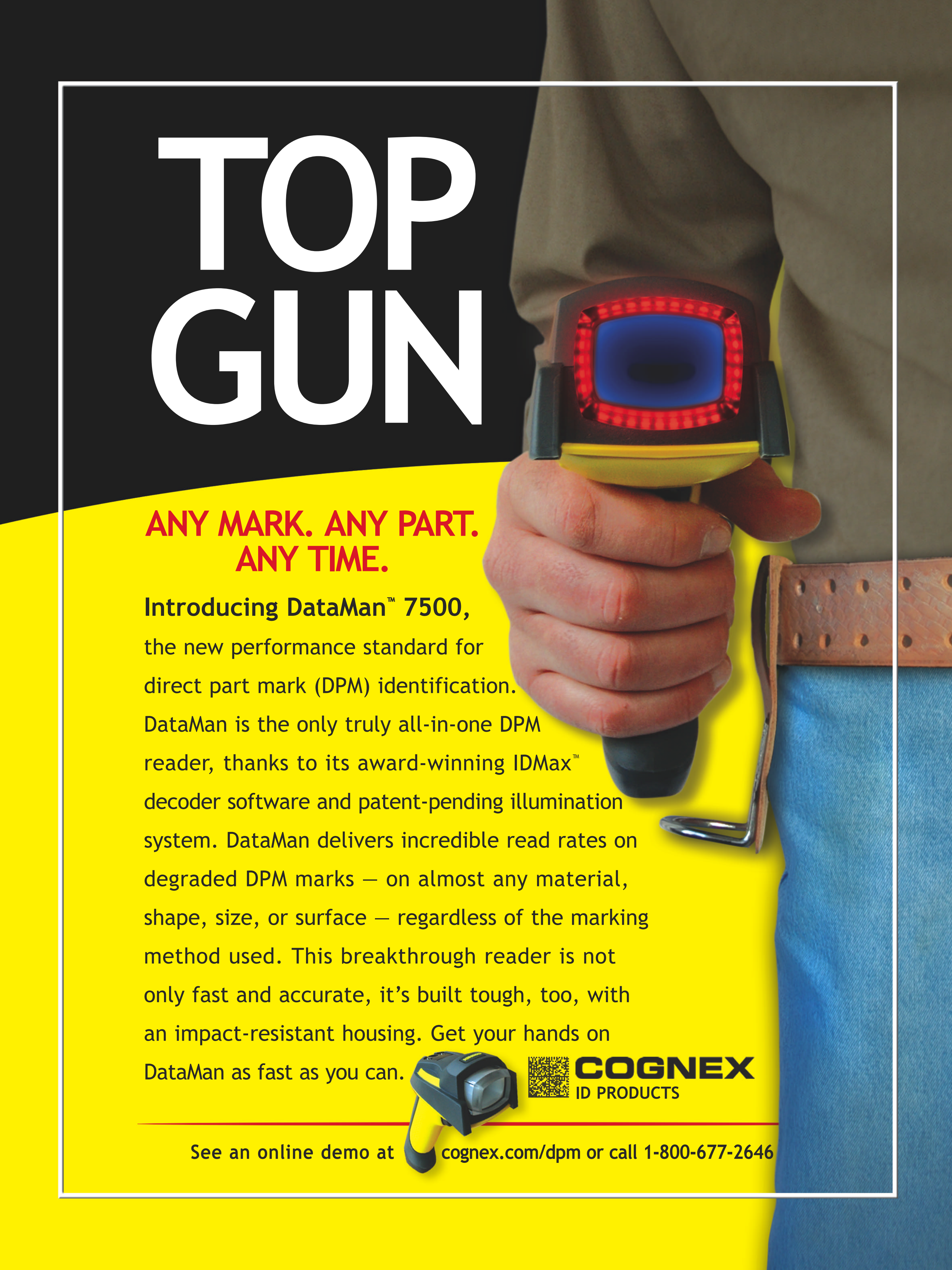
The latest update to the standard calls for incorporating power into the Camera Link cable, which would eliminate the need for a special power cable. Although the idea has been well received, some manufacturers have expressed concern over backward-compatibility. The current proposal before the committee—scheduled for final action by May of this year—accepts the concept, provided that prior-generation nonpowered equipment would incur no damage because of the change.

The mini-connector currently includes four ground pins at the corners of a rectangle, and the new version would convert two of those to power pins. The remaining ground pins would serve as the connector's inner shield. To maintain compatibility, a powered frame grabber would detect nonpowered equipment or cable faults out on the line before applying power. Camera manufacturers would include a resistance of between 50 Ω and 200 kΩ on the powered lines to assist the protection logic.

According to Kinney, Camera Link minimizes component count, reduces power consumption, and remains the most straightforward camera-to-frame-grabber communication standard to implement. It "is the lowest-cost, highest-performance solution for connecting video components," he said. Many OEM and military applications already require Camera Link compliance.

GigE Vision standard emerges

As with Camera Link, developers of the GigE Vision standard recognized the bandwidth, scalability, networking, and processing-flexibility limitations of standards such as FireWire (IEEE



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Camera Link and GigE • from page 53

1394b) and USB for real-time applications. The developers based their standard on Gigabit Ethernet (GigE), which overcomes those limitations.

"It seemed an ideal fit for real-time machine-vision applications," said George Chamberlain, president of Pleora Technologies and former co-chair of the GigE Vision committee. "It had plenty of bandwidth and supported a wide range of networking and processing architectures—including distributed processing and pipeline processing—using standard PCs and switches. It wasn't a daisy chain configuration, either. It offered dedicated, full-duplex connectivity over either copper or fiber, so there was no bandwidth sharing between links, which is important for real-time operation. And 10GigE, the next generation, will support transmission speeds of 10 Gbps, more than enough for evolving throughput requirements."

The goal of the GigE Vision committee, which began its work in 2003, was to standardize communications over GigE for vision applications from the camera head all the way to the target application. "We wanted to promote software and hardware interoperability independent of vendor. This would reduce support requirements and shorten time-to-market for OEMs who incorporate compliant products into their systems," said Chamberlain. "The idea was to deliver a framework that would support low-cost as well as high-value cameras without imposing excessive restrictions on their designs." Chamberlain contends that GigE, along with the emerging GigE Vision standard, stands to benefit both manufacturers and users of machine-vision equipment by reducing the cost and complexity of the final application.

Publication is imminent

The first version of the GigE Vision standard, now almost finished, is expected to be released by the Automated Imaging Association (AIA) in mid-2006. Although the standard does not discuss applications, and thereby offers manufacturers a broad latitude, it nevertheless addresses traditional machine-vision applications that must deliver high-speed image data. The standard includes four basic elements:

- The GigE Vision Control Protocol (GVCP)—which runs on top of UDP (Universal Datagram Protocol) IPv4—defines how to control and configure compliant devices (such as cameras), specifies stream channels, and provides mechanisms for cameras to send image and control data to host computers.
- The GigE Vision Stream Protocol (GVSP) defines data types and describes how images are transmitted over GigE.
- The GigE Device Discovery Mechanism defines how cameras and other compliant devices obtain IP addresses.
- An XML description file based on the emerging GenICam standard developed by the European Machine Vision Association (EMVA) provides the equivalent of a computer-readable datasheet to allow access to camera controls and image streams.

With regard to GenICam, Chamberlain commented, "The GigE portion of the standard fulfills its original goals. GenICam, however, places constraints on camera design that are inconsistent with the implementation style of many camera manufacturers."

GigE transports data in "packets" to any network-connected device. A packet consists of a specified set of bits containing a header, a payload, and a trailer (**Figure 3**). The header includes information about the data stream that will follow, ensuring that the packet is assembled, prioritized, transmitted, and received in accordance with the OSI model on which the standard is based. The data stream itself represents the transmission payload. The trailer provides information required for error-checking, ensuring that error-free data arrives at the receiving end.

Chamberlain said that the GigE Vision standard offers advantages over Camera Link. It can, for example, transmit low-latency sustained video data up to 100 m without repeaters—and can transmit it further with low-cost GigE switches or optical-fiber

Camera Link and GigE

from page 55

cable. GigE Vision uses industry-standard PC and LAN equipment—such as GigE network interface cards or network-interface chips (NICs) in place of specialized frame-grabber boards—which reduces the resulting network's complexity and implementation costs. Making use of commercial software reduces costs further.

The 1-Gbps data rate of GigE translates to an image transfer rate of up to 115 Mbytes/s, which supporters contend meets 90% of today's image-transfer requirements. Full-duplex (bidirectional) data transfers enable users to control cameras or video devices like any other IP-connected network devices. GigE Vision also supports a wide range of networking options, including single camera to single PC, multiple cameras to a single PC, a single camera to multiple PCs, and multiple cameras to multiple PCs.

Header				Payload	Trailer
64 bits	48 bits	48 bits	16 bits	46 to 1500 bytes	32 bits
Preamble	Destination address	Source address	Type/ length	Data	Frame check sequence (CRC)

Fig. 3 All Ethernet packets consist of headers, payloads, and trailers. Courtesy of Pleora Technologies.

Comparing the alternatives

Table 1 compares GigE, Camera Link, FireWire, and USB 2.0. In raw speed, Camera Link comes out the winner, easily accommodating high-performance vision applications. It can stream data at rates up to 6.12 Gbps over dedicated point-to-point copper links of 10 m or less. The 10-m maximum, however, requires tethering PCs to cameras or incorporating repeaters or more expensive fiber-optic cable. Another drawback: Camera Link isn't flexible enough for interconnecting several cameras or for centralizing control and maintenance. Because it runs over specialized cables and terminates on PCI frame grabbers, the standard enjoys few economies of scale.

FireWire, on the other hand, which evolved for consumer applications, offers "plug-and-play" capability, and uses a readily available low-cost PC interface. With its bus topology, up to 63 devices share 800 Mbps (up to 512 Mbps for a single camera) in a "daisy chain." Adjacent devices can be separated by up to 4.5 m to a maximum of 72 m over twisted-pair copper cable.

FireWire does not, however, include error-checking algorithms, and its relatively limited bandwidth must be shared among all cameras on the network. In addition, FireWire's Windows driver monopolizes the PC during data transfer. (Some manufacturers have addressed this by developing proprietary drivers.) The cost of its copper cable represents another drawback. Less expensive options are available, but at a considerable sacrifice in bandwidth.

Like FireWire, USB also developed as a standard for connecting peripherals to PCs. As such, it can deliver up to 480 Mbps, much slower than either GigE or Camera Link, and the bandwidth must be shared among up to 127 connected devices. Its chief advantage rests in its ubiquitousness, but it lacks sufficient power to succeed in most inspection-imaging applications.

In addition to data packets, a GigE Vision system includes two other key elements—the camera interface and the physical infrastructure. All GigE video or imaging cameras must include an Ethernet interface. It provides full-duplex (bidirectional) data, allowing image data to flow from the camera to the PC as control data flows from the PC to the camera. System integrators can implement the interface in two ways. An IP/Ethernet communications software stack can run on a microprocessor with an embedded operating system. Chamberlain contends that at high data rates, typical implementations of such systems can consume as much as 25 W of power at GigE's full data rate. Thus, this approach serves best in low-performance applications.

Alternatively, a manufacturer can develop hardware that contains hard-coded packet-processing functions that eliminate the embedded operating system. This approach packetizes data with clock-cycle accuracy, delivering latencies as low as 500 µs. It also consumes much less power—less than 2.25 W in some implementations—and more easily integrates into cameras.

Clearly, of the currently available options, GigE and Camera Link exhibit distinct advantages over the more consumer-oriented USB and Firewire 1394b. Still, they both present benefits and drawbacks. In the end, as always, application needs will dictate which transport framework to use. □

Table 1. A comparison of the vision standards for inspection applications.

	GIGE	CAMERA LINK	FIREWIRE	USB
Type of standard	Commercial	Commercial	Consumer	Consumer
Connection type	Point-to-point or LAN	Point-to-point	Peer-to-peer	Master-slave
Bandwidth	<1000 Mbps	Base: 2.040 Mbps Med: 4.080 Mbps Full: 6.120 Mbps	<800 Mbps (but only 512 Mbps for image data)	<12Mbps, USB1.1 <480 Mbps, USB2
Topology	Link	Link	Bus	Bus
Cabling	RJ-45, Cat-5 (4 x twisted pair)	MDR-26-pin for Camera Link	4/6-pin STP	4-pin STP
Camera interface	External adapter or built-in	Built-in	Built-in	Built-in
PC interface	GigE NIC	PCI frame grabber	PCI card	PCI card
Data transfer type	Dedicated	Dedicated	Asynchronous/isochronous	Asynchronous/isochronous
Streaming video	Continuous	Continuous	Burst	Burst
Distance Max. with switches Max. with fiber optics	<100 m no limit no limit	<10 m no limit no limit	<4.5 m (full bandwidth) 72 m 200 m	<5 m 30 m Not available
Wireless support	Yes	No	No	No
Max. # of cameras	Unlimited	1	63	127
Full-duplex mode	Yes	Yes	Yes	Yes
Network control	Yes	No	Yes	No
I/O control	RS-232 or GPIO	Yes	Yes	Yes
Real-time signaling	No	Yes	No	No
Virtual link support	Yes	No	Yes	No
Area-scan support	Yes	Yes	Yes	Yes
Line-scan support	Yes	Yes	Limited	No
Multi-camera support	Yes	Yes*	Yes	No
Windows driver	Native or proprietary	Proprietary	Native	Native

**Camera Link supports multiple cameras only with multiple frame grabbers or with a multi-port frame-grabber configuration.*

Sources: Pleora Technologies and JAI Pulnix.

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PRODUCTS

AOI system

Viscom's S6056 not only performs automatic optical inspection of printed-circuit boards (PCBs) but also offers the option of parallel inspection to double throughput. For parallel inspection, the system is fitted with a double track and two sensor modules, permitting the simultaneous inspection of two PCBs per transport lane. An integrated shuttle is available for the twin-track, both on the input side as well as the output side, thereby eliminating the need for external switching points for use in single-line production. *Viscom, www.viscom.de.*

GigE-enabled frame grabber

Useful for applications where the host computer cannot be located near a camera, the X64-CL GigE Lite bundles X64 frame grabber and Gigabit Ethernet technologies in a stand-alone box to capture images from a Camera Link area-scan or line-scan camera and transfer them over a Gigabit Ethernet link to a PC. Camera controls are localized on the X64-CL GigE Lite, while data is streamed at rates of up to 1 Gbps over point-to-point connections of 100 m per network segment. *Dalsa Coreco, www.dalsa-coreco.com.*

AOI system with LED source

Rohde & Schwarz has added a complex-array LED source to the Laser-Vision family of AOI systems. Manufactured by Schneider & Koch, the systems use diagonally arranged LED lighting units coupled with LED ring lighting from above. The light source enables the system to capture images, monitor the position of components, and check features such as soldered joints, polarities, or short circuits. The diagonally arranged lighting highlights object corners and features to permit detection of black components on dark printed-circuit boards. *Rohde & Schwarz, www.rohde-schwarz.com.*

Measurement sensor

The ZS smart measurement sensor from Omron combines two-dimensional CMOS imaging with laser measurements to create an inspection system that provides 110-μs response time and 0.25-μm resolution for inspecting moving work pieces and capturing data on the fly. The sensor's gain setting can be customized for specific environmental conditions. Five sensor heads are available, for distances ranging from 20 to 200 mm and measuring ranges from ±1 to ±50 mm. Prices: amplifier—$1450; sensor heads—$2450 to $3450. *Omron, www.omron.com/oei.*

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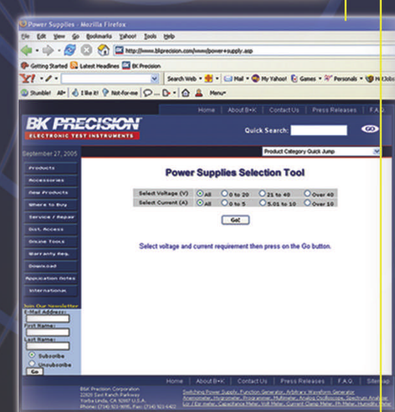

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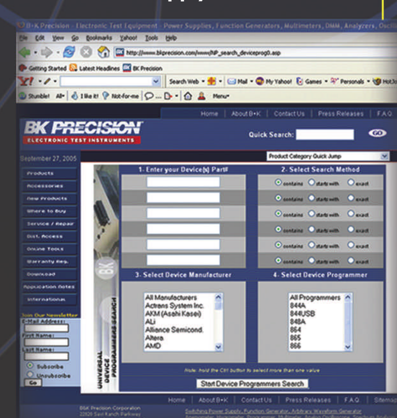

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A PXI horse for the RF course

Rick Nelson, Chief Editor

In October 2003, Aeroflex began offering PXI products for testing mobile phones and components such as RFICs. The company now offers a family of PXI modules that combine to form RF signal generators and analyzers operating to 6 GHz. In November 2005, Aeroflex released software suites for PXI-based test of WLAN and GSM/EDGE products.

I spoke with Tim Carey, Aeroflex's product manager for PXI test systems, about PXI's applicability to RF applications.

Q What is Aeroflex's strategy with regard to software suites?

A Our software addresses gaps in the market. Development environments like LabView and LabWindows offer a wide variety of functions that can be applied to acquired data. But they don't address the needs of some of the 2G, 3G, and 4G communications standards that are fueling the demands for RF test equipment. So, we have developed measurement libraries that can be used in any development environments that support COM or ActiveX standards.

Q What prompted Aeroflex to look at PXI?

A. Our reasons were threefold. First, we needed a product architecture that was modular and reusable across Aeroflex. Having some core technology that is reusable throughout the company is paramount to improving time to market for new development. Second, we recognized that our customers' test-system development requirements would be similar to our own in that they need to accelerate time to market, which is best addressed by the flexibility and reuse of modular instrumentation. The final reason was cost. Test-system costs were escalating in line with the complexity of parametric test cases in design verification and production. We saw PXI as a good compromise for making very complex measurements at reasonable cost.

Q What are the prospects for PXI vs. LXI?

A Aeroflex supports the LXI standard, with LXI and PXI representing alternative approaches to the same problem. It's very much horses for courses.

Q Does the new PXI Express spec have ramifications for RF test?

A For any real-time measurement application where signal bandwidth is large or the event record is long, PXI Express will help accelerate test time. We are at the moment not able to stream our data in real time across the PXI backplane. With PXI Express, the possibilities for us to be able to communicate our full bandwidth data either in real time or near real time increase significantly. Now, we rely for real-time applications on our own LVDS front-panel interfaces, which provide the advantage of not being compromised by any Windows interrupts or backplane bottlenecks.

Q Are there any technical limits of the PXI platform that limit the maximum frequency at which PXI instruments can operate?

A No, nothing inherent in the PXI standard limits the frequency range. If you looked inside any of our other microwave instruments, they are to a larger or lesser extent modular. Nothing precludes that being engineered in PXI. It is the case that higher-frequency instruments tend to be heavier, usually because of the amount of RF screening. We did find in our initial development of RF modular instruments that being constrained to the 3U PXI form factor led to elegant and efficient designs. □

The 3030A digitizer operates from 330 MHz to 3 GHz with a 33-MHz digitized bandwidth, while the companion 3035 operates to 6 GHz with a 36-MHz digitized bandwidth.

Courtesy of Aeroflex.

Tim Carey provides more details on PXI products, performance, cost, and hardware and software compatibility in the online version of this article: www.tmworld.com/0206_pxi.

INSIDE *this issue*

EDITOR'S NOTE

PXI targets performance

Rick Nelson, Chief Editor

Conventional wisdom has it that modular instruments can enable you to build flexible, economical test systems, yet you'll need rack-and-stack GPIB equipment for optimal performance. That's no longer the case, if it ever was.

As evidence of benchtop performance in modular form factors, both National Instruments and Signametrics announced 7½-digit DMM cards for the PXI bus last year. In the RF arena, Aeroflex continues to expand its lineup of PXI source and digitizer hardware and software products, which top out at 6 GHz. And the company sees no inherent limitations to upping PXI instrument bandwidth when the market warrants that move. Furthermore, the advent of PXI Express is making possible the real-time transfer of test data to a central processing unit.

There are still good reasons you may not want to do that. In some cases, a self-contained box that makes measurements and processes data might be your most cost-effective choice, especially if you prefer local processing using a real-time operating system or DSPs. That can be valuable in evaluating whether a component meets a particular wireless communications standard, for instance. But with PXI on the scene, you'll need to evaluate your options. The odder the job you face or the wider range of chores you must contend with, the more likely you'll want the flexibility to reconfigure hardware and software test resources that modular systems provide. □

Contact Rick Nelson at rnelson@tmworld.com.

NEWS

Geotest gets USAF contract

GEOTEST-MARVIN Test Systems has announced that it has been awarded a contract by the US Air Force for the purchase of 26 MTS-206 Maverick Missile field test sets. The MTS-206 is a rugged, portable PXI-based test set with built-in support for all Maverick components.

With the MTS-206, Maverick users can test all versions of the AGM-65 missiles, missile sections, launchers, and missile-launcher clusters. The MTS-206 logs all parametric test results and maintains an electronic log of all assemblies tested. "The MTS-206 is yet another proof that PXI is now a mainstream platform for military applications," said Loofie Gutterman, president of Geotest. www.geotestinc.com. □

Booklet covers PXI Express

PICKERING Interfaces has published the 4th edition of *PXImate*, a booklet explaining PXI hardware and software basics. The new edition includes an overview of the emerging LXI and PXI Express standards. Topics covered range from power-supply routing through measurement of intermodulation and RF mixer parameters. The booklet is free, but registration is required. www.pickeringtest.com. □

PXI tester has military applications

ADVINT HAS introduced its Puma ruggedized PXI test system for factory-to-field support of military and industrial electronics. The company also announced that the tester is currently fielded by multiple branches of the US military and is in use by various prime contractors.

The Puma provides an open-architecture platform for functional testing of a variety of digital, analog, and RF electronics and avionics subsystems and systems. It supports organizational-, intermediate-, and depot-level test activities.

The Puma employs a single-frame, 19-in. rack-mount system that contains 3U 18-slot PXI and four-slot SCXI chassis and an array of COTS instrumentation. The system uses National Instruments LabWindows/CVI and LabView test programs under the control of NI's TestStand test-management software. The Puma comes with power distribution, UUT power supplies, UUT isolation, and system cooling. It uses MacPanel's Series L2000 interface test adapters to provide a high-density, compact interface to the UUT. www.advint.com. □

ADLINK opens European office

ADLINK TECHNOLOGY has opened an office in Dusseldorf, Germany, which will offer products and services based on CompactPCI and PXI technologies for industrial computers. "The European office will focus on reinforcing long-term partnerships with distributors located around the continent as well as providing local support to our European customers," said Jim Liu, CEO of ADLINK. www.adlinktech.com. □

Seminar covers PXI

THE PXI SYSTEMS Alliance (PXISA) has announced the 2006 PXI Technology and Application Conference, a seminar that will tour 15 North American cities this spring. The free, full-day event presents an introduction to the PXI specifications, case studies, hands-on technical training, and guidelines for PXI system integration.

The event will debut on March 28 in Dallas and will visit several US cities, as well as Toronto, Juarez, and Tijuana, before concluding in Boston on June 15. www.pxitac.com. □

STANDARDS

PXI Express raises throughput, adds differential clocking

Rick Nelson, Chief Editor

The PXI Systems Alliance (PXISA) published the PXI Express specification last August, and you can expect to see PXI Express instruments coming to market this year. With those instruments, you will be able to take advantage of a 45-fold increase in bandwidth—to 6 Gbytes/s, vs. 132 Mbytes/s for what's now called PXI-1.

PXI Express leverages the widely adopted PCI Express specification, and PXI Express modules will comply with the CompactPCI Express standard, which combines the PCI Express electrical specification with rugged Eurocard mechanical packaging and differential connectors (see "PXI Express spec paces PICMG effort," p. 66). PXI Express offers mechanical and electrical interoperability with CompactPCI Express products, so as new CompactPCI Express products are introduced, systems will support both PXI Express and CompactPCI Express modules.

Hybrid slots

In addition, you will be able to use PXI Express modules along with more than 1000 existing PXI modules. Chassis that support PXI Express will continue to have 32-bit PXI-1 slots. The PXI Express standard also defines hybrid module slots that will accommodate existing modules as well as emerging Express-class instruments.

For example, the standard defines 3U hybrid peripheral slots that have three connectors: P1, XP3, and XP4, where P1 carries 32-bit PCI signals; XP3 is dedicated for PCI Express data lines, differential triggers, and timing signals; and XP4 carries the timing and synchronization signals defined in the PXI-1 specification. The 6U hybrid peripheral slot defined in the PXI Express standard adds an XP8 connector to provide additional power to 6U modules.

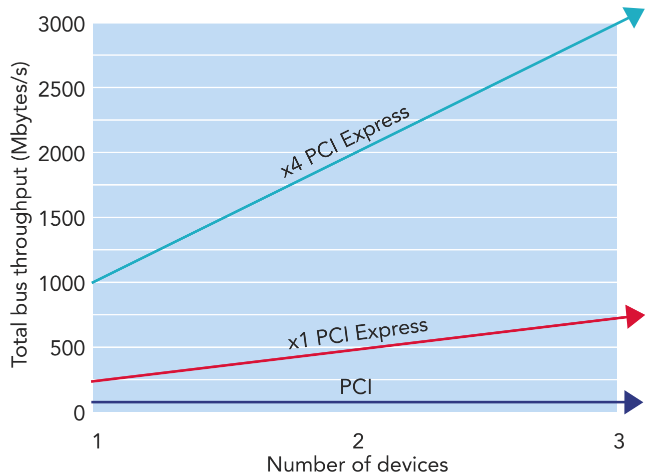

Fig. 1 Traditional PCI implementations share the available 32-bit, 33-MHz bandwidth among all connected devices; PCI Express, and hence PXI Express, offer dedicated bandwidth per device.

As you add PXI Express modules to your instrument systems, you'll be able to take advantage of new PXI Express instrumentation features including a new differential 100-MHz system clock, differential synchronization, and differential star triggering. The new differential functions will offer enhanced noise immunity and low jitter at higher clock frequencies.

Furthermore, the higher-speed clocks can eliminate the need for costly clock multiplication circuits in emerging PXI Express instruments while maintaining compatibility with existing PXI-1 modules, because the new 100-MHz clock is phase-aligned with the 10-MHz clock of the existing PXI-1 spec, according to the specification (Ref. 1).

Dedicated bandwidth

Darcy Dement, senior product manager for modular instruments at National Instruments, emphasized that the top-line benefit of PCI Express is its high, scalable bandwidth. She pointed out that, unlike PXI-1, whose 132-Mbytes/s bandwidth must be shared among all the peripheral devices on any given segment, PCI Express, and hence PXI Express, offer dedicated bandwidth per device, so total bus throughput actually increases with the number of connected devices (**Figure 1**).

Who needs all that bandwidth? High-bandwidth IF instruments for communications test systems (see "A PXI horse for the RF course," p. 61); high-channel-count, high-sample-rate data-acquisition systems; and high-speed image-acquisition systems are among the applications often cited as ones that can benefit from PCI Express and PXI Express.

Richard McDonell, PXI group manager at National Instruments, commented, "Since the PXI Express spec was approved back in August, we've been contacted by a number of instrument vendors as well as non-instrument vendors who have been building their own ruggedized proprietary architectures, and they are seriously considering PXI Express. So, it's not only opened up opportunities for existing applications to run even faster, but it has also opened up appli-

PXI Express • from page 65

cations that we would never have dreamed could move to a COTS environment," adding that he can't disclose specifics at this time.

Dement cited as a specific example a demonstration at NIWeek 2005 in which a table-saw monitoring application (Ref. 2) involved the real-time synchronization of a saw-blade image with acquired saw load, rotational speed, and two-axes vibration data (**Figure 2**). In this application, the 320-Mbytes/s image-data transfer far outstrips the capacity of the traditional PCI bus. Although the NIWeek demo was implemented in PCI Express modules residing in a desktop PC, the emergence of PXI Express offers the opportunity to extend this or similar applications to take advantage of star triggering and other PXI-specific functions.

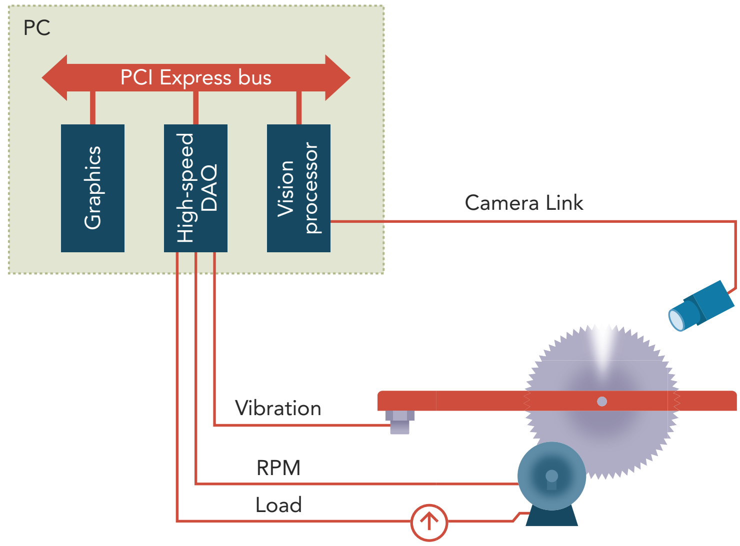

Fig. 2 Hinting at PXI Express capabilities, a demo at NIWeek 2005 involved acquisition of a table saw's load, speed, and two-axis vibration data for synchronization with image data, acquired over a Camera Link interface. This demo was implemented using desktop-PC-resident PCI Express cards.

Preserving software

Dement explained that as you move to PXI Express, you can preserve your software investment. The PCI Express standard, she said, "provides for complete software compatibility between PCI and PCI Express down to a very low level. For example, about a year ago, we released a GPIB interface for PCI Express, and we didn't have to change a single line of code in our own PCI driver to support the PCI Express interface." The PXI Express standard (Ref. 3) affords the same level of compatibility.

As you wait for PXI Express to arrive, Dement said you can take advantage of PXI Express-level bandwidths using already available PCI Express instrument modules, and you can even link them to existing PXI-1 systems. To do that, you can employ a MXI-Express interface in a desktop computer having PCI Express slots, or you can use ExpressCard MXI in conjunction with a laptop.

But the wait shouldn't be long. McDonell won't put a date on the first PXI Express product debuts from National Instruments, but such introductions "are a priority on our part." The main issue, he explained, was just getting the PXISA spec nailed down. Now that that's happened, he said, "We've already got many PCI Express-based cards and PXI modules shipping, so we have in-house expertise in both architectures to get the first wave of PXI Express products out there." □

PXI Express spec paces PICMG effort

THE PXI SYSTEMS ALLIANCE'S August 16 announcement of the new PXI Express specification came on the heels of the August 9 public announcement of the CompactPCI Express specification by PICMG (www.picmg.org), the consortium founded in 1994 as the PCI Industrial Computer Manufacturers Group. CompactPCI Express brings PCI Express technology to the PICMG 2.0 CompactPCI form factor, while maintaining compatibility with CompactPCI hardware and software.

PICMG now includes more than 450 companies; it collaboratively develops open specifications for telecommunications and industrial computing applications. Participating in the CompactPCI Express specification development process were more than 40 of those companies, whose goal was to meet the future market needs of the CompactPCI, PXI, military, and aerospace markets. The specification defines the connector, electrical, and mechanical requirements of 3U/6U system boards, peripheral boards, switch boards, and backplanes based on the rugged IEEE 1101 Eurocard mechanical packaging standard. —*Rick Nelson*

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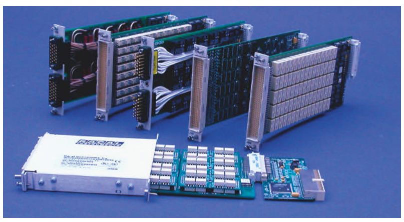
2. Slockers, Shawn, and Brent Roberts, "High-Bandwidth DAQ Systems," NIWeek 2005 Video Presentation, National Instruments, www.ni.com/niweek/keynote_videos.htm#niw.

3. PXI Express Software Specification, Revision 1.0, August 31, 2005, PXI Systems Alliance, www.pxisa.org/specs.htm.

PRODUCTS

PXI product line

Building upon its product line used in VXI, GPIB, and Ethernet testing environments, EADS North America Defense Test & Services now offers 11 switch and four digital I/O Adapt-a-Switch PXI modules. Employing a PXI



carrier designed by Racal Instruments, these modules can be used in a PXI chassis without modification.

EADS North America Defense Test & Services was formed in 2004 when EADS combined its Access Research and Racal Instruments subsidiaries. The company now offers four versions of the Racal Instruments 1260-1114 high-density digital I/O modules that provide 96 TTL, CMOS, or OC (open-collector) I/O lines or 48 high-voltage/high-current OC I/O lines. EADS also offers seven versions of the 1260-1145 high-density switch matrix, which provides passive monitoring of up to 144 cross points and can serve in automotive system-level testing.

The new line-up also includes the 1260-1138A, a 64-channel, two-wire scanner/multiplexer; the 1260-1150, which offers a 500-MHz bandwidth and bidirectional electromechanical I/O; the 1260-1118 80-channel, 2-A, 300-VAC/VDC, 100-MHz SPST switch module; and the 1260-1120 20-channel SPST switch with individual 10-ADC/13-AAC switch ratings.

Base prices: $945 to $2675. *EADS North America Defense Test & Services, www.racalinstruments.com.*

3U digitizers

The Acqiris dual-channel DC152 and single-channel DC122 10-bit 4-Gsamples/s 3U digitizers are designed to reduce testing and data-acquisition time for high-speed applications such as telecommunications and semiconductor testing. Input bandwidths up to 3 GHz make these digitizers suitable for replacing standard multimeters, oscilloscopes, power meters, and frequency counters in synthetic instrumentation systems. The digitizers comply with the PXI and CompactPCI standards and are supported with AcqirisLive and AcqirisMAQS software as well as Windows, Linux, and VxWorks drivers for easy integration into automatic test equipment. *Acqiris, www.acqiris.com.*

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PXI resistance simulator card

Used for automotive resistance simulation, the PXI 4009 programmable resistance decade card provides two resistance channels and covers a resistance range of 0 to 1 MΩ with a resolution of 0.5 Ω. You can program a complete resistance sweep via the driver. The PXI 4009 includes onboard memory for storing calibration data and works in both PXI and CompactPCI systems. *Goepel Electronics, www.goepel.com.*

20-slot, 3U PXI chassis

The GX7300 20-slot, 3U PXI chassis features one system controller slot and 19 PXI/CPCI slots, accommodates optional built-in peripherals (including a hard drive and CD-ROM), and is available with an 800- or 1100-W power supply. In addition, the GX7300 features an onboard microcontroller, which provides per-slot temperature monitoring and automatic shut down of the system if an over-temperature condition occurs. *Geotest, www.geotestinc.com.*

RF/microwave converters

Ascor, a division of Giga-tronics, has introduced a range of RF and microwave upconverters and downconverters that extend the frequency range of the National Instruments PXI 5660 RF analyzer and PXI 5671 digital signal generator from 2.7 GHz to 6 GHz. Three types of converters are available: 4.9- to 6-GHz block converters, 2.7- to 6-GHz tunable converters, and 3.2- to 4.2-GHz block converters. Each is available in up, down, or up/down configurations. *Ascor, www.ascor.com.*

Low-cost oscilloscope

Available in PCI and PXI configurations, the ZT450-10 addition to the ZT450 family of digital storage oscilloscopes offers two-channel, 500-Msamples/s, 250-MHz performance for $2995. The module provides features typically found in bench oscilloscopes, such as flexible signal conditioning, advanced triggering, multiple acquisition modes, and onboard signal processing. It supports software, pattern, pulse-width, and video triggering with independent trigger sources for channels A and B; trigger inputs are accessible via the front panel or the local-bus backplane. *ZTEC Instruments, www.ztec-inc.com.*

Test & Measurement World

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PRODUCTUPDATE

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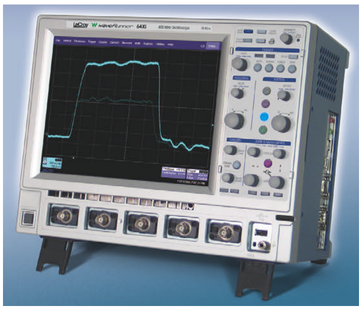
Scope family gets larger screen

LeCroy's WaveRunner Xi series of oscilloscopes takes its small footprint from the Wavesurfer line while adding increased specifications and features. The WaveRunner Xi comes in three models: one 400-MHz version (four channels, $8500) and two 600-MHz versions (two or four channels, $7500 and $10,000). All models sample at 5 Gsamples/s, with the 600-MHz models interleaving channels to get 10 Gsamples/s. All models provide 2 Msamples/channel of waveform memory.



With its 6-in. depth and its 10.4-in. touch-screen display, the scope consumes little bench space. It even comes with a screen pointer and a place to store it.

Among the features now available in the upright form factor is fast-viewing with color-gradient displays. The scope updates the screen 8000 times/s. The triggers now operate at the scope's full bandwidth. I/O buses include USB and Ethernet, with IEEE 488 optional.

Options include a 32-channel logic probe, CAN bus triggering and decoding, power measurements, jitter measurements, digital filtering, disk-drive measurements, and up to 24 Msamples of waveform memory. *LeCroy, www.lecroy.com.*

OTN test platform

Innocor adds OTU1 test capabilities to its OTN TestPoint offering to address the needs of transport applications that require FEC and OTN Digital Wrapper testing at the 2.666-Gbps line rate. With this new capability, TestPoint now supports four FEC line rates: 10.709, 11.049, 11.095, and 2.666 Gbps. The OTU1 test option is available as a factory upgrade to the Multi-Rate module for the TestPoint TS-10, TS-30, and TS-170 configurations. *Innocor, www.innocor.com.*

Voice/video/data test set

Housed in a convenient handheld package, the CoLT-450 modular test set lets service providers verify VoIP, Video over DSL, and DSL services such as ADSL2+, ADSL, SHDSL, and VDSL. The Video-over-DSL Test Suite option allows the battery-operated CoLT-450 to display the video streaming rate and any MPEG2/4 or WM9 errors, IP packet loss, ADSL and ATM frame losses, and errors for the previous 5 min using an on-screen time reference marker. Testing does not require an external DSL modem, set-top box, or TV. *Consultronics, www.consultronics.com.*

Matlab API for WLAN tester

The LitePoint Matlab API software package provides a Matlab-compatible interface to the analysis and command resources found in the IQview IEEE 802.11a/b/g WLAN test platform. This wide-bandwidth single instrument is capable of performing all 802.11a/b/g transmitter and receiver tests with its integrated VSA and VSG functionality, including MIMO and optional Bluetooth V1.1, 1.2, and 2.0 with EDR. Price: $5995 for a single-user license, including one year of product updates. *LitePoint, www.litepoint.com.*

Pocket PC-based virtual instrument

Virtins Pocket Instrument modular software uses the sound chip in a Pocket PC to turn your handheld computer into a real-time oscilloscope, spectrum analyzer, and signal generator. The oscilloscope module offers a selectable sampling frequency of up to 96 kHz, sampling bit resolution of 8 or 16 bits, and one or two channels. The spectrum analyzer module lets you view amplitude spectrum and phase spectrum, while the signal generator supports multitone generation where you can combine up to 32 tones in each channel. It also provides arbitrary waveform generation through a user-defined waveform library. The software bundle costs $49.95. Modules can also be purchased separately. *Virtins Technology, www.virtins.com.*

Linux drivers

Extending Linux support to over 200 devices, National Instruments offers NI-DAQmx 8 driver software for PCI, PCI Express, and PXI-bus-based instruments, including data-acquisition, signal-conditioning, dynamic-signal-acquisition, and switching hardware. Additional NI instrument drivers for Linux accommodate digital multimeters, high-speed digitizers, arbitrary waveform generators, and instrument-control devices. NI-DAQmx 8 is available free of charge and supports ANSI C and LabView 8 programming languages. *National Instruments, www.ni.com.*

Multiple-port RS-232 communication card

Contained on a universal PCI 2.2 card, the PCI-1610AJU furnishes four RS-232 ports with built-in RJ-45 connectors to simplify wiring. The card's small size and convenient RJ-45 connectors make it particularly useful for ATM installations. Its universal interface allows operation in both 3.3-V and 5-V environments, and it is the first Advantech serial communication card to support Windows XP Embedded. Price: $125. *Advantech, www.eautomationpro.com/us.*

Deep-memory scopes

Agilent expands its Infiniium line of oscilloscopes with four digital storage and mixed-signal models, two each at 600-MHz and 1-GHz bandwidths. All of the scopes come with four analog channels, while two models add 16 logic inputs for debugging mixed-signal systems. Each instrument samples at 4 Gsamples/s on two channels (2 Gsamples/s on four channels) with standard waveform memory of 1 Msample/channel on two channels and 500 ksamples/channel on four channels. Optional memory is available up to 128 Msamples (64 Msamples/channel on four channels). Price range: $14,895 to $22,995. *Agilent Technologies, www.agilent.com.*

1500-W switching supplies

Housed in a low-profile 8x11x2.5-in. enclosure, the 1K5U series of switching power supplies accepts a universal 90-VAC to 260-VAC input and provides high-current single outputs ranging from 12 VDC to 60 VDC. Output voltages are adjustable by either a potentiometer or external controls. The power-factor-corrected units meet harmonic current standard EN61000-3-2,3 and worldwide safety certification standard EN60950. Standard features include remote sense, forced current sharing for parallel operation, power fail signal, and comprehensive overvoltage, short-circuit, and over-temperature protection. Price: $598 (100 units). *Power Sources Unlimited, www.psui.com.*

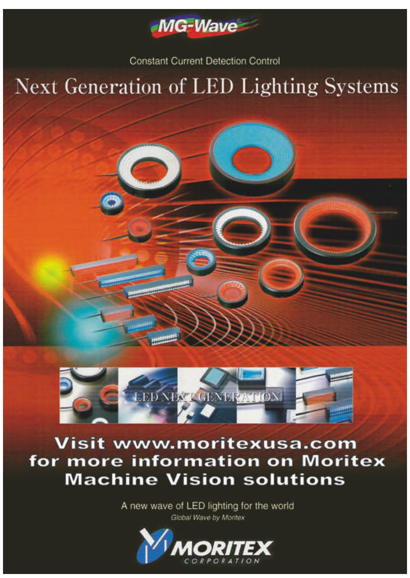
Thermocouple probes

KMQXL and NMQXL Super OmegaClad XL quick disconnect probes come in K and N thermocouple calibrations for temperature measurement up to 1335°C (2440°F). Nickel chrome-based Super OmegaClad sheathing provides very low drift at high temperature. The probes are available with grounded, ungrounded, or exposed thermocouple junctions and sheath lengths of 6 in. and 12 in. Base price: $27. *Omega Engineering, www.omega.com.*

Programmable switcher

The newest member of the Genesys family of programmable switching power supplies delivers 3.3 kW of output power from a 19-in., 2U package. Models are available with output voltages up to 600 V and output current to 400 A. Digital and isolated analog interfaces are optional. *Lambda Americas, www.lambda-emi.com.*

▷ Visit **www.tmworld.com/webproducts** for additional product write-ups.



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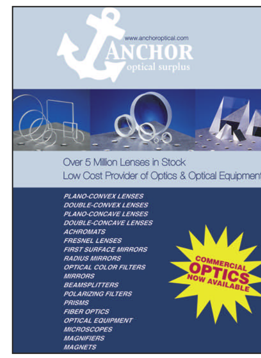

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VIEWPOINT

[An exclusive interview with a technical leader]

PATRICK T. FLYNN
President
Everett Charles Technologies
Pomona, CA

Patrick Flynn became president of Everett Charles Technologies (ECT) in May 2005, after previously heading the company's Capital Equipment and Services Group and Semiconductor Test Group. Joining ECT in 2000, Flynn has been instrumental in leading key product introductions, as well as the firm's expansion into Asia.

His 25 years of experience in technology management include executive positions in the aerospace, automation, and motion-control industries. Flynn was the first American to receive a Marcus Wallenburg Foundation Fellowship to attend MIT, where he earned an MS in management.

To some, the broad product mix at ECT might suggest lack of focus. But as Flynn sees it, this diversity creates a prime vantage point for viewing the emerging needs of test engineers.

Benefits from the "big picture"

Q: How does ECT stay in tune with what customers want?

A: We keep a close watch on strategic customers to understand their products as well as the markets they serve. Because ECT goes all the way from semiconductors to loaded board test, we get good insights on where electronics test is headed. So, we really have a good window on the future, and that allows us to stay ahead of the curve on our own product developments.

Q: What other steps do you take to foster innovation?

A: Innovation is a key part of our corporate culture, and it all starts with this question: How can we help customers solve their test problems? We have process review committees that bring together technical specialists, sales, marketing, operations, and manufacturing. This is the forum we use to analyze market trends, the technologies required to meet customer needs, and what it will take to manufacture these products.

Q: Can you give an example of a product that reflects this process?

A: A good example is the Eliminator PCB test cell. As you know, printed-circuit boards are becoming more and more complex. Yet companies need to test these boards in a cost-effective way. With Eliminator, you don't need test fixtures, which can be very difficult and costly to build. The Eliminator can test a 24x24-in. panel in less than 2 min, regardless of the number of images per panel, test pitch, density, or test point count. Eliminator also shines in package test, where it can test very fine geometries without expensive test fixtures. With this product, customers can determine what voltages they want to test at—up to 250 V. With high voltage, customers can do a very thorough job of test and more easily pinpoint defects on a board.

Q: What about product breakthroughs in semiconductor test?

A: A key area is testing MEMS devices. This is a fast expanding technology that includes air-bag, ABS, tire-pressure, and rollover sensors, and even drop sensors for PC notebooks. Our German IC handler company, Multitest, has developed some unique approaches for delivering MEMS devices to the test contactor. In flip testing, for example, we make the module that flips the MEMS chip.

Q: You seem to be getting some big orders for flying-probe test systems.

A: Much of that trend can be traced to lot size. It used to be that a board shop might build thousands of a particular product. Now, they build them in lots of 200, 100, or even less. With these flying-probe systems, no tooling or fixtures are required. You get the data, create a program for the tester—and off you go. It's a system that is well tailored for small lots and for cutting cycle time.

Q: How do you achieve zero defects in your products?

A: It really comes down to our ability to get quality data from our customers, which can be a big challenge. Customers have distinct preferences, so we try to set up defaults in our products tailored not only to a company, but to specific engineers and specific testers within that company. This requires a tremendous focus on customer relations.

A useful tool that we rely on—ProWorks—keeps this detailed data in a central repository. This makes it easier for a new ECT engineer coming onto that job to understand a customer's needs. It all relates to throughput. We are a part of the customer's revenue stream. If we can't deliver the test interface they need in a timely fashion, we aren't helping them. T&MW

The online version of this article includes more Q&A with Patrick Flynn on probes, technologies for loaded PCBs, and ECT's global plans. www.tmworld.com/2006_02.

You need this clock generator

CG635 – Precise, low jitter clocks from DC to 2.05 GHz

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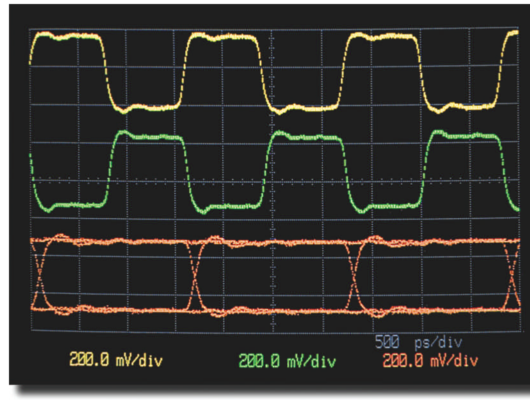
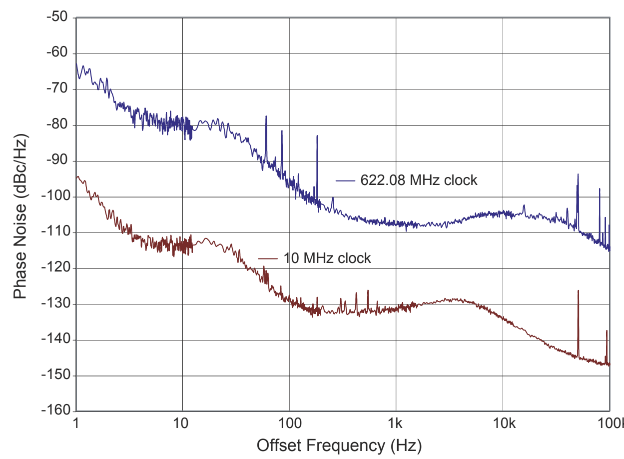


Clock and PRBS signals at 622.08 MHz

Plot shows complementary clock and PRBS (opt. 1) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).



Phase noise for 10 MHz and 622.08 MHz outputs

- ***Square wave clocks from DC to 2.05 GHz***
- ***Random jitter <1 ps (rms)***
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- ***16-digit frequency resolution***
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The CG635 Synthesized Clock Generator provides square wave clocks between DC and 2.05 GHz that are clean, fast and accurate. With jitter less than 1 ps, transition times of 80 ps, and 16 digits of frequency resolution, the CG635 will meet your most critical clock requirements.

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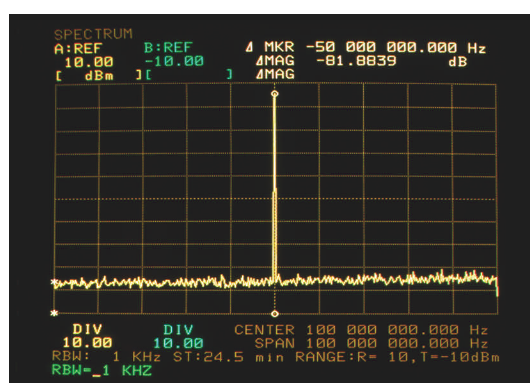
Whether you are trying to lower the noise floor of an ADC, increase SFDR of a fast DAC, or squash the bit error rate in a SerDes, the CG635 is the tool you need to get the job done.



RF Spectrum of a 100 MHz clock

Graph shows a 100 MHz span around a 100 MHz clock. Only two features are present: the clock at 100 MHz, and the spectrum analyzer's noise floor (around –82 dBc).

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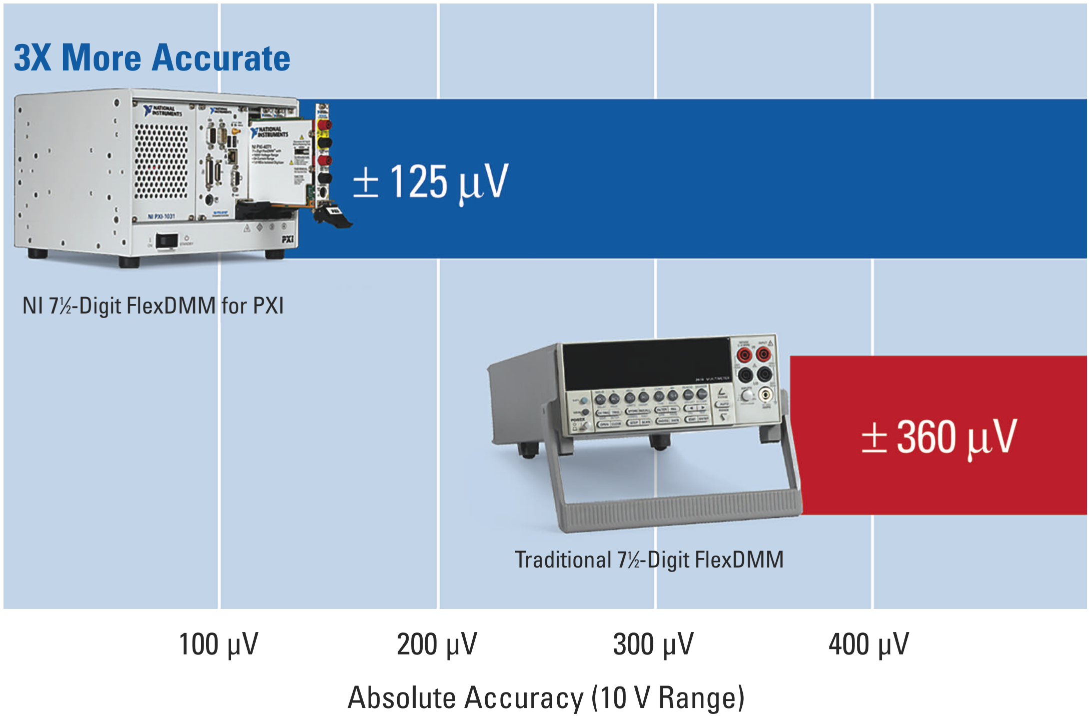

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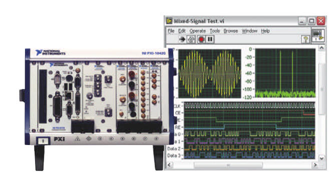

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